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SYSTEMATIC EVALUATION OF METAL GATE ELECTRODE EFFECTIVE WORK FUNCTION AND ITS INFLUENCE ON DEVICE PERFORMANCE IN CMOS DEVICES

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Dedication

To my loving family

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As the CMOS integrated circuits are reduced to the 100-nanometer regime, the conventional SiO_2-based gate dielectrics are facing serious scaling challenges. High-k materials are expected to replace SiO_2 as the gate insulator. However, metal gates are coherently needed to replace poly-Si due to the increase in threshold voltage for high-k stacks with poly-Si gates and the poly depletion effect. The challenge in metal gate research is to obtain metals with effective work function (EWF) values of ~5.0-5.2eV for p-MOS and 4.1-4.3eV for n-MOS. Although EWF should be determined predominately by the vacuum WF of the materials, it is observed that the EWF is different on high-k than on SiO_2. One proposed mechanism to limit the EWF tuning on high-k dielectrics,

and a possible inherent roadblock to the identification of band-edge metals, is the Fermi-level pinning effect

Metal gate EWF has been systematically studied with the goal of identifying band-edge metal gate electrode candidates. The terraced oxide technique has been developed as the metric for accurate EWF extraction. A comparison of the literature Fermi-level pinning models with our experimental data shows that an intrinsic limitation (pinning at the high-k charge neutrality level) may not exist and the source of most EWF deviation on high-k is due to extrinsic contributions, such as interfacial reactions. Both the bulk metal characteristics and the interface properties between the metal and dielectric have been found to control overall EWF. Charges can be induced in the gate stack during device processing and shift the flatband voltage (V_{fb}). Engineering of the EWF by an interface dipole has been identified as a plausible approach for EWF tuning. Aluminum-containing electrode stacks and lanthanide electrode stacks are proposed as potential p-type and n-type metal candidates.

The potential impact of candidate metal systems on device performance and reliability was studied, as well as other materials that may reveal implications for the influence of the electrode on the gate stack. Comparison of the deposition techniques, shows that even physical vapor deposited (PVD) metal electrodes can exhibit high performance. Metals with high O reactivity will reduce the high-k and consequently degrade electron mobility. No long term reliability concerns were observed for the candidate metals.

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CHAPTER 1

INTRODUCTION AND BACKGROUND

1.1 CHALLENGES TO TRANSISTOR SCALING

1.1.1 Challenges for Moore's Law

In the evolution of the electronics industry, downscaling of the metal oxide semiconductor field effect transistor (MOSFET) dimensions has been one of the key driving forces for gains in performance and productivity as predicted by Moore's law [1]. For the past few decades, reduction in device size has enabled the increased number of transistors per chip with enhanced circuit functionality and performance at lower cost (Figure 1.1). Physical scaling of dielectric had been the approach to enhance drive current. However, as devices approach the sub 100 nm scale, traditional silicon dioxide dielectrics used in the transistor stack have been pushed to the physical limit (Figure 1.2) and exhibit high leakage currents. Therefore, an alternative material solution is needed to enable the further scaling. To achieve the target performance for the 65nm technology node and beyond, the effective oxide thicknesses (EOT) of material stacks are required to scale <1nm. Dielectric films with a higher dielectric constant (high-k) are identified as a plausible solution to achieve the same capacitance (same EOT) while maintaining a relatively thicker physical thickness [2]. Hafnium based high-k dielectrics are the preferred material system for its thermal stability with the Si substrate, and appropriate κ value 16~25 [3, 4]. Since the band-gap of dielectrics tend to be inversely proportional to their dielectric constants, high-k films will have lower band-gap and result in smaller barrier heights. A sufficient barrier height is needed to suppress leakage currents.

Therefore, Hf based dielectrics (HfO_2, $HfSiO_x$, $HfSiO_xN_y$)with band gap of ~5.7eV are optimum dielectrics.

1.1.2 Motivation for metal gate electrodes

Performance and reliability issues remain concerns for the implementation of high-k dielectrics, however key roadblocks are issues involving interaction between the polysilicon (poly-Si/poly) electrode and high-k. An unfavorable increase in the threshold voltage (V_t) have been observed for poly/high-k devices, especially for the p-type MOS (pMOS) devices (nMOS V_{tn} increase ~0.4eV; pMOS V_{tp} increase ~0.7eV) [5]. The Fermi-level pinning phenomena [6-8], suggests the Fermi-level of the poly-Si is easily pinned to the energy level of metal oxide surface states due to charge exchange between the electrode and the dielectric. Sources of such surface states may be, for Hf-based dielectrics, the presence of Si-Hf bonds, or oxygen vacancies (oxygen deficient interfaces). The pinning location is believed to be just below the Si conduction band (~0.3eV below conduction band edge of Si), and thus explains the different V_t increase for n/pMOS (Figure 1.3)[8, 9]. Another limitation to the use of poly-Si gates is the poly depletion effect. It occurs when the MOSFET is turned on and the poly gate electrode is depleted at the poly/dielectric interface. This thin depletion layer adds to the EOT (~3-4 Å) and consequently, reduces the gate capacitance and drain current [10]. As the EOT target goes down, this additional layer cannot be neglected. These scaling challenges have lead to the use of metal gate electrodes to replace poly-Si gates [11]. Metal gate electrodes have the advantage of reducing poly/high-k interaction, eliminating poly depletion, as well as reducing B penetration from the doped poly-Si into the gate dielectric, and gate resistance. However, there has been limited consensus on the appropriate electrode material, with production ready performances.

Alternatively, the industry has sought to the use of nitrided oxides with strain engineered channels to improve carrier mobility, and has detoured off the scaling approach for enhance device performance (90nm, 65nm nodes) [12]. However, the limitations to poly/nitrided oxide stacks still remains, and metal electrodes in conjunction with or without high-k dielectrics still remain a critical technology solution for sub-32nm node applications.

1.2 REQUIREMENTS OF THE METAL GATE TECHNOLOGY

The quest for alternative metal electrodes faces several challenges in both device characteristics and process integration. The optimal electrode material should exhibit 1) proper work functions, 2) thermal/chemical stability with the underlying dielectric and 3) ease of process integration.

1.2.1 The effective work function (EWF) of metal gate electrodes

Gate work functions suitable for bulk complementary MOSFET (CMOSFET) devices are simulated to be near the band-edge of Si to achieve suitable V_t for maximized drive current [13]. Therefore, metal work function values should be~5.0-5.2eV for p-MOS, and 4.1-4.3eV for n-MOS. "Effective work function (EWF)" of metal gates is the term used to describe the metal work function in a MOS stack. It is traditionally characterized by forming MOS capacitors with varying oxide thickness and measuring the flat band voltage, V_{fb}, as a function of oxide thickness (Figure 1.4). The work function is extracted from the V_{fb}-EOT relationship which ideally follows the following equation [14]:

$$V_{fb} = \Phi_{ms} - \frac{Q_f}{\varepsilon_{ox}} \cdot T_{ox}$$

Φ_{ms}: work function difference between gate and substrate
Q_f: fixed oxide-silicon interface charge density
ε_{ox}: dielectric constant of the insulator
T_{ox}: equivalent oxide thickness

The electrode work function is then determined using Φ_{ms} and the known work function of the silicon substrate (Φ_s), as shown in Figure 1.5.

EWF should be predominately determined by the bulk/vacuum work function of the materials, which is mostly determined by the electronic and ionic structure of the metal. The bulk (vacuum) work function for materials in the periodic table is reported by Michaelson et al. (Figure 1.6)[15]. Materials in columns IIIB, IVB and VB are suitable for n-type EWF, while materials in column VIII have p-type EWFs. Reports of the EWF of various metal gate materials on SiO_2 have followed the bulk work function reasonably (Figure 1.7) [16-21]. However, the lack of direct correlation suggests other factors besides the bulk work function also impact the EWF (such as interfacial reaction [22], film structural changes [23, 24], etc.). The factors controlling EWF of metal electrodes on high-k dielectrics (namely Hf-based dielectrics) exhibits a higher level of complexity. From the thermal stability concerns of metals on high-k, the deposition process variation (film thickness) [25, 26] and influence of bulk/interface charges from the dielectric itself [27], the extracted EWF based on the linear V_{fb}-EOT relationships have shown a great disparity even for a single metal system(Figure 1.8).

Summary of reported literature EWF values for various metal electrodes is shown in Appendix I. They can be conveniently categorized into groups such as pure metals (Al, Zr, Hf, Ti, Ta, Mo, Co, Pd, Ni, Re, Ir, Ru, Pt, W etc.), bi-metal alloys (RuTa, NiTi, PtTa etc.), metal nitrides (binary metal nitride: WN, TiN, TaN, MoN; ternary metal nitride systems: TaSiN, TiSiN, TiAlN etc.), conducting metal oxides (RuO_2, IrO_2 etc.) and metal silicides (NiSi, CoSi, TiSi, HfSi, WSi etc.). Elemental metals have exhibited near band-edge work functions, and binary metal alloys allows tuning of the work function by controlling the composition of the alloy. Addition of a nitrogen or Si component to the metal in most cases is reported to shift the work function toward mid-gap (4.6~4.8eV).

It has also been shown that not only the metal electrode itself, but also extrinsic contributions from the overall gatestack used in the fabrication of the devices, as shown in Figure 1.9, will impact the extracted EWF. Such complexity has obstructed the identification of band-edge metal electrode systems, and the understanding of EWF control on high-k dielectrics.

1.2.2 Thermal stability of metal electrodes

Considering the conventional gate-first process integration, the metal gate material not only needs to have the correct work function, and low resistivity, but it should be thermodynamically stable with its surrounding materials, especially the gate dielectric [19]. Electrical properties will be affected with annealing conditions if a reaction occurs, such as change in EOT, threshold voltage or gate leakage current. Interdiffusion or chemical reactions are mostly attributed to the difference in the electronegativity and atomic radii of the materials. A thorough thermal stability study of various elemental metals and metal compounds on SiO_2 and Al_2O_3 gate dielectrics had been conducted by C. Cabral, Jr. et al. by in-situ XRD [28]. It is found that elemental metals with n-MOS work functions undergo reactions with the dielectric, while others become unstable due to its low melting point. Agglomeration is the issue in most of the p-MOS compatible materials. Physical and electrical properties of metal gate electrodes (TiN, TaSiN, WN, TaN, TaSi, Ir, IrO_2) on HfO_2 had been studied by J. Schaeffer et al. in which material and interface studies elucidate which classes of metal gates are promising dual metal electrodes candidates [29]. From their study, mostly ternary/binary metal nitrides satisfy the thermal stability requirements of metal gates.

In the screening process for candidate electrode materials, detailed understanding of the atomic characteristics of these metals are essential. Appendix II shows the

summarized material characteristics (bulk work function values, melting point, resistivity, expansion coefficient, electronic specific heat) of several materials, as well as the diffusion coefficient/activation energy, or diffusivity at 1000^{o}C in Si, which will be important parameters in the integration process. The electrical capture cross section, and electron/hole trap energy levels of these materials in Si is also essential in determining minority carrier lifetime if the gate metal diffuses within the channel. The gate etch process for metals is an critical module in metal gate integration. Information of available compound formation for these metals can provide directions for dry-etching solutions [30].

1.3 CHALLENGES TO THE METAL GATE TECHNOLOGY

1.3.1 Identification of suitable band edge work function electrodes

Identification of suitable band edge work function electrode materials is the key challenge to the metal gate technology. However, due to the complex nature of the metal/high-k interface, minimization of error in the EWF study is needed to enable systematic study of factors impacting work function. Unlike SiO_2, using the traditional V_{fb}-EOT extraction with various thickness of high-K is shown to exhibit error in the EWF up to 0.3eV and may contribute to the disparity in the literature EWF results in Figure 1.8 (More discussion can be found in Chapter 2). Therefore, an standardized EWF extraction technique needs to be established first for accurate EWF extraction on high-k.

Although identification of suitable WF materials may be possible, a roadblock in implementing proper work function electrodes on high-k has been proposed [6, 31-33]. The Fermi-level (E_f) pinning effect now between metal/high-k suggests EWF on high-k would be different from its bulk value, vary with the underlying dielectric, and exhibit a

smaller range for EWF tuning than SiO_2 (Figure 1.10)[6]. The metal induced gap states (MIGS) model has been proposed to be the key intrinsic component inducing E_f-pinning. The MIGS model suggests electrodes in contact with a dielectric will induce virtual states in the dielectric, and interfacial charge transfer will shift the metal E_f towards the charge neutrality level of the dielectric. It also predicts in order to achieve 5.2eV EWF on HfO_2, the electrode needs to have a bulk WF larger than 5.5eV, which only one element in the periodic table (Pt) qualify, significantly limiting the chances of a p-type EWF solution. And yet EWF results in the literature from pure Pt still has limited application to pMOS [34, 35]. Multiple efforts to apply the MIGS theory to explain experimental results have shown good correlation [6, 36], while other results cannot be completely addressed with this model [33, 37]. Due to the limited consensus, a systematic study of the existence of an intrinsic EWF limit is needed.

1.3.2 Study of metal electrode's impact on device performance

The initial goal of obtaining band edge EWF metal gate was to enable EOT scaling with maximized drive current, therefore it is crucial to study the impact of electrodes on transistor device performance. Reports have shown the use of metal gate electrodes is effective in screening phonon scattering in the high-k dielectric, which they believe is the primary reason for mobility degradation in high-k films. Metal gate limit phonons from coupling to the channel under inversion conditions, and thus result in improved channel electron mobility [38]. Narayanan et al. [39] reported that electron mobility optimization is critically dependent on specific electrode and interface layer combinations as well as post deposition processing for the high-k films. Specific chemistry for chemical deposition of the gate electrode, as well as the presence of N both influence the reliability and performance of the device. The impact of metal gate process

on the high-k gate stack have been reported in [40, 41] which the different charge trapping characteristics observe between ALD/PVD processes is from its influence on the high-k bottom interface. The study of device performance and reliability for the candidate metal stacks require careful investigation of mobility, V_t leakage current, and gate stack changes due to the metal electrode. Combined with physical analysis, to investigate sources of metal's influence. The goal is to identify key process and material influences, and hopefully will provide insight into the choice of candidate metal electrode material systems and identify potential roadblocks.

1.4 DISSERTATION OUTLINE

A standardized method for work function measurement named the "terraced oxide" method is proposed in Chapter 2. Comparison of the EWF extracted based on this capacitance based measurement (C-V) and the barrier height between the metal/high-k dielectric (based on a leakage current method) is performed to validate the accuracy of the extraction. Various material systems will be evaluated utilizing this extraction technique.

In Chapter 3, the critical question of whether there is intrinsic limitation to achieving band edge EWF metals on high-k is addressed based on terraced oxide results and correlation to the MIGS model.

A systematic breakdown of detailed understanding of factors contributing to the EWF of metal electrodes and the possible control/engineering of these factors to our benefit is discussed in Chapter 4.

Utilization of the understanding in Chapter 4, engineering the metal/high-k interface in end allows band-edge EWF to be achieved with interface engineering.

Identified n-type and p-type electrode candidates and their EWF mechanisms are discussed in Chapter 5.

Chapter 6 is the evaluation of the device performance of band edge metals, combined with physical analysis to understand the influence of metal gates on device properties, and furthermore, the influence of metal gates on device reliability.

Finally, chapter 7 discusses a new phenomena which is presented to be limiting the integration of p-type EWF metals at low EOTs. Therefore, utilization at the 32nm node still faces its challenges, and suggested approach for future studies are proposed.

1.5 FIGURES

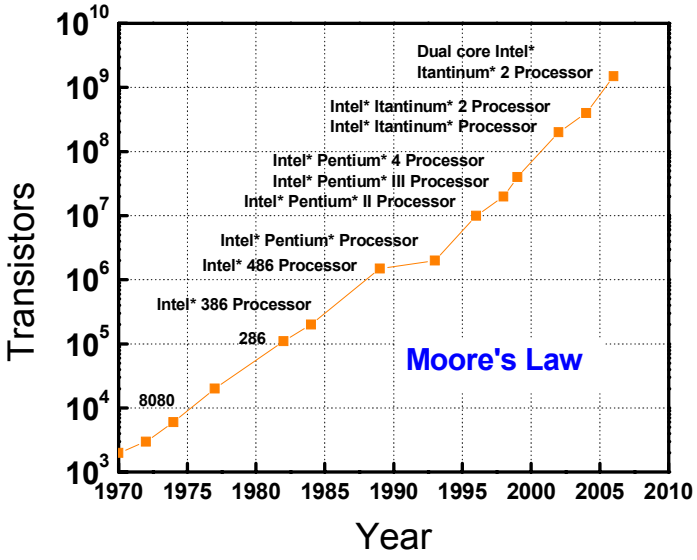

Figure 1.1 **Moore's Law Means More Performance. Processing power, measured in millions of instructions per second (MIPS), has steadily risen because of increased transistor counts [1].**

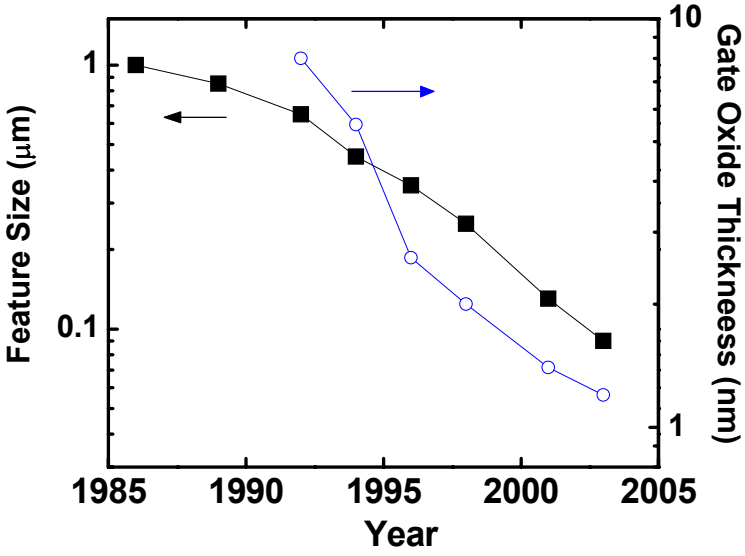

Figure 1.2 **Feature size of transistors in Intel processors decreases exponentially over time and the gate oxide thickness decreases accordingly [1].**

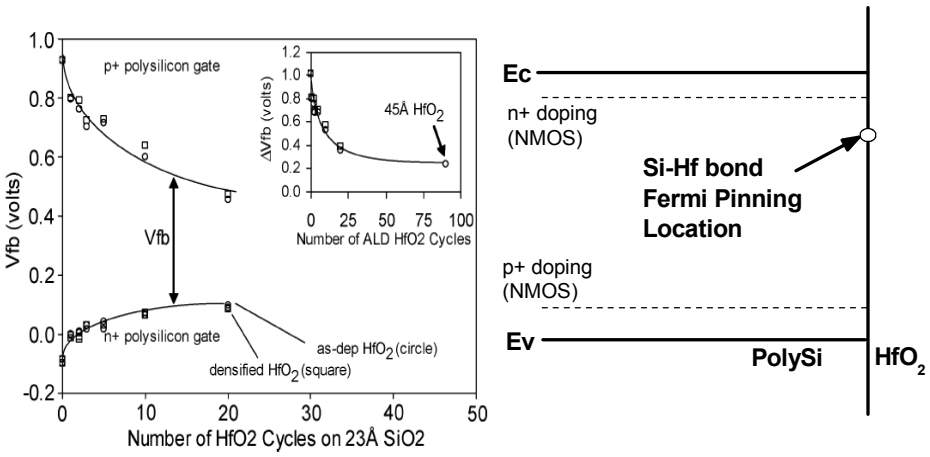

Figure 1.3 **Flatband voltage versus number of HfO_2 ALD cycles. (Inset: ΔV_{fb} versus number of HfO_2 ALD cycles) from reference [8]. Schematic of Fermi pinning location with respect to Si conduction and valence bands. (C. Hobbs et al., IEEE TED, v.51, p.978, ©2003 IEEE)**

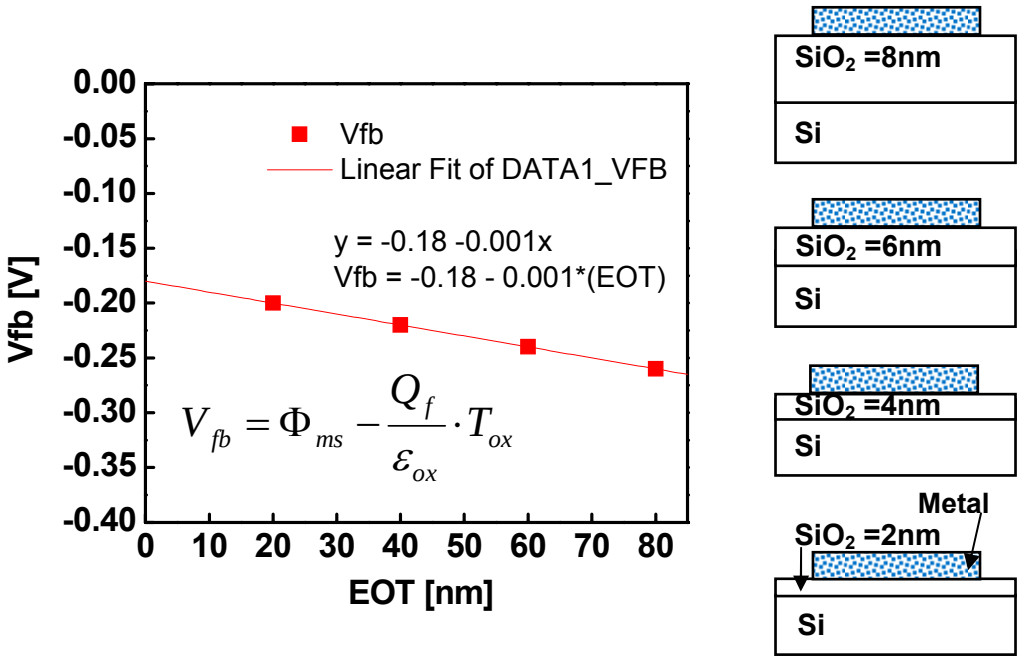

Figure 1.4 **EWF extraction from linear V_{fb}-EOT relationship measured on thickness series of SiO_2.**

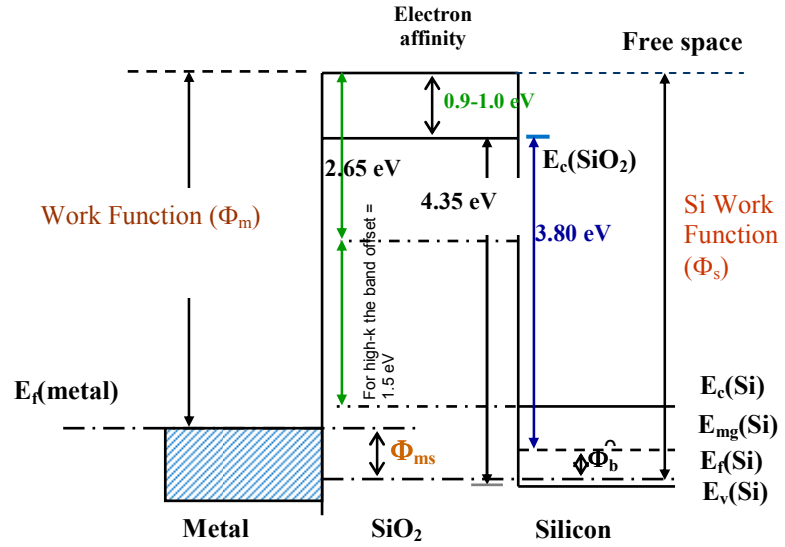

Figure 1.5 Band diagram of work function alignment in metal/dielectric/Si system at flat band condition.

IA	IIA	IIIB	IVB	VB	VIB	VIIB		VIII		IB	IIB	IIIA	IVA	VA	VIA	VIIA
3 Li 2.9	4 Be 4.98											5 B 4.45	6 C 5.0			
11 Na 2.75	12 Mg 3.66											13 Al 4.28	14 Si 4.85	15 P · · ·	16 S · · ·	
19 K 2.30	20 Ca 2.87	21 Sc 3.5	22 Ti 4.33	23 V 4.3	24 Cr 4.5	25 Mn 4.1	26 Fe 4.5	27 Co 5.0	28 Ni 5.15	29 Cu 4.65	30 Zn 4.33	31 Ga 4.2	32 Ge 5.0	33 As 3.75	34 Se 5.9	Br
37 Rb 2.16	38 Sr 2.59	39 Y 3.1	40 Zr 4.05	41 Nb 4.3	42 Mo 4.6	43 Tc · · ·	44 Ru 4.71	45 Rh 4.98	46 Pd 5.12	47 Ag 4.26	48 Cd 4.22	49 In 4.12	50 Sn 4.42	51 Sb 4.55	52 Te 4.95	I
55 Cs 2.14	56 Ba 2.7	57 La 3.5	72 Hf 3.9	73 Ta 4.25	74 W 4.55	75 Re 4.96	76 Os 4.83	77 Ir 5.27	78 Pt 5.65	79 Au 5.1	80 Hg 4.49	81 Tl 3.84	82 Pb 4.25	83 Bi 4.22	84 Po · · ·	At
87 Fr · · ·	88 Ra · · ·	89 Ac · · ·	90 Th 3.4	91 Pa · · ·	92 U 3.63											
			58 Ce 2.9	59 Pr · · ·	60 Nd 3.2	61 Pm · · ·	62 Sm 2.7	63 Eu 2.5	64 Gd 3.1	65 Tb 3.0	66 Dy · · ·	67 Ho · · ·	68 Er · · ·	69 Tm · · ·	70 Yb · · ·	71 Lu 3.3
			90 Th 3.4	91 Pa	92 U 3.63	93 Np	· · ·	· · ·	· · ·	· · ·	· · ·	· · ·	· · ·	· · ·	· · ·	· · ·

Figure 1.6 Vacuum work function of elements shown in the periodic table from [15]. (Reprinted with permission from H. Michaelson, JAP, v. 48, p. 4729, Copyright 1977, American Institute of Physics)

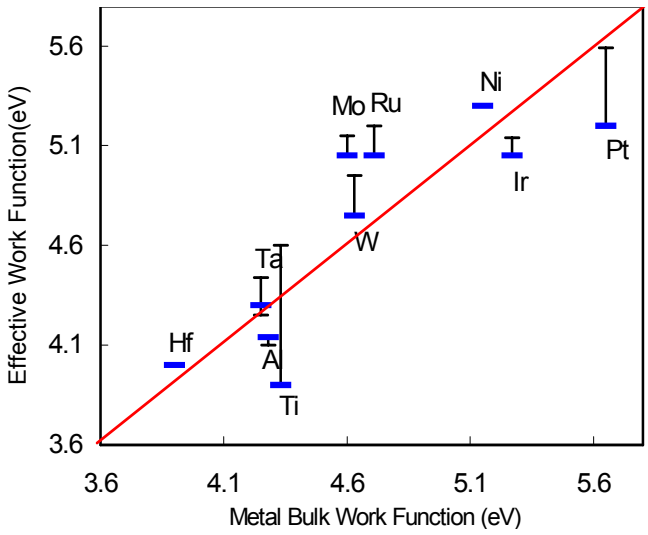

Figure 1.7 Effective work function on SiO_2 versus bulk work function for various metal electrodes reported in the literature.

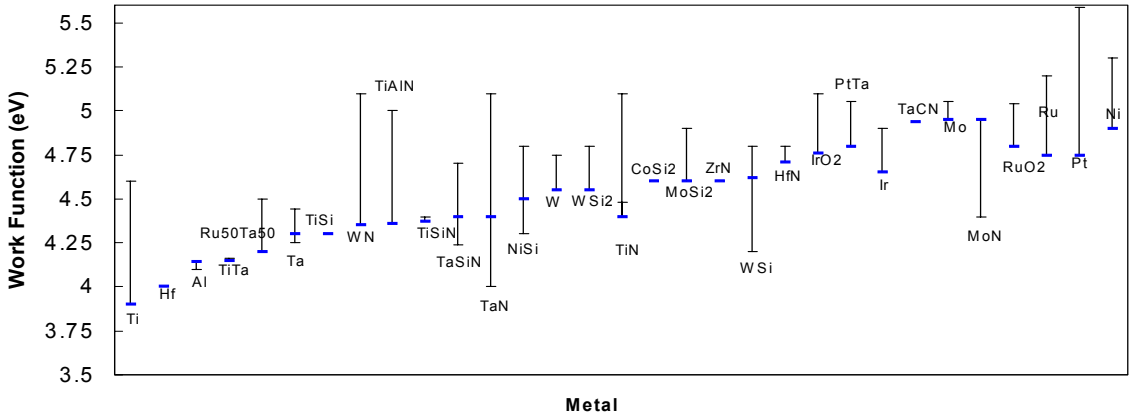

Figure 1.8 Effective work function of various metal electrodes on HfO_2 reported in the literature showing disparity in reported values even for a single material system.

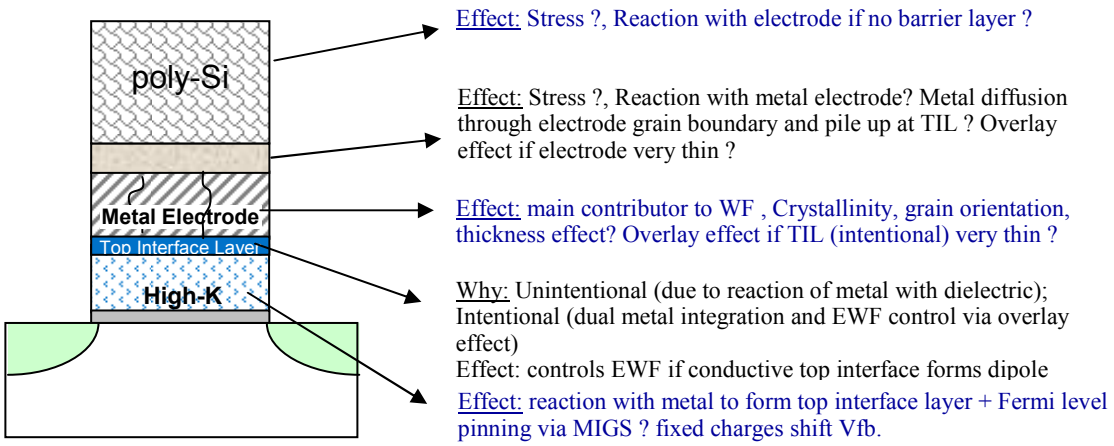

Figure 1.9 Diagram of MOSFET gate stack and their influence on EWF

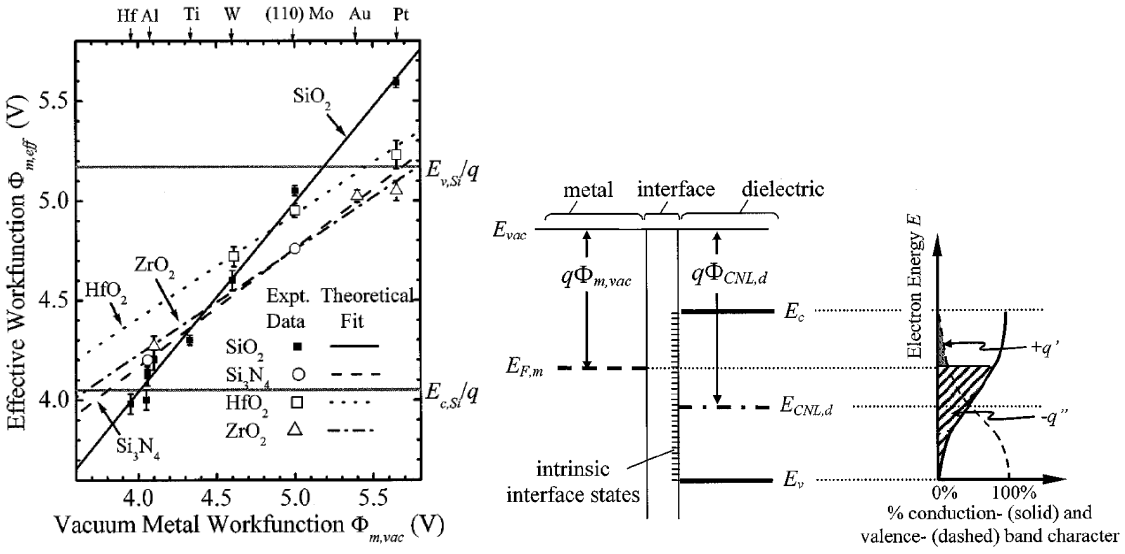

Figure 1.10 Predicted EWF values from MIGS model compared to experimental results, and the schematic showing band diagram of interface changed states. [6] (Reprinted with permission from Y. eo, JAP, v. 92, p. 7266, Copyright 2002, American Institute of Physics)

1.6 REFERENCES

[1] G. E. Moore, "Progress in digital integrated electronics," presented at Electron Devices Meeting, 1975 International, 1975.

[2] G. D. Wilk, R. M. Wallace, and J. M. Anthony, "High-k gate dielectrics: Current status and materials properties considerations," *Journal of Applied Physics*, vol. 89, pp. 5243-5275, 2001.

[3] B. H. Lee, L. Kang, W.-J. Qi, R. Nieh, Y. Jeon, K. Onishi, and J. C. Lee, "Ultrathin hafnium oxide with low leakage and excellent reliability for alternative gate dielectric application," presented at Electron Devices Meeting, 1999. IEDM Technical Digest. International, 1999.

[4] L. Kang, B. H. Lee, W.-J. Qi, Y. Jeon, R. Nieh, S. Gopalan, K. Onishi, and J. C. Lee, "Electrical characteristics of highly reliable ultrathin hafnium oxide gate dielectric," *Electron Device Letters, IEEE*, vol. 21, pp. 181-183, 2000.

[5] C. Hobbs, L. Fonseca, V. Dhandapani, S. Samavedam, B. Taylor, J. Grant, L. Dip, D. Triyoso, R. Hegde, D. Gilmer, R. Garcla, D. Roan, L. Lovejoy, R. Rai, L. Hebert, H. Tseng, B. White, and P. Tobin, "Fermi Level Pinning at the PolySietal Oxide Interface," *VLSI Technology Digest*, pp. 9-10, 2003.

[6] Y. C. Yeo, T. J. King, and C. M. Hu, "Metal-dielectric band alignment and its implications for metal gate complementary metal-oxide-semiconductor technology," *Journal of Applied Physics*, vol. 92, pp. 7266-7271, 2002.

[7] S. Samavedam, L. B. La, P. J. Tobin, B. White, C. Hobbs, L. R. C. Fonseca, A. Demkov, J. Schaeffer, E. Luckowski, A. Martinez, M. Raymond, D. Triyoso, D. Roan, V. Dhandapani, R. Garcia, S. G. H. Anderson, K. Moore, H. H. Tseng, C. Capasso, O. Adetutu, D. C. Gilmer, W. J. Taylor, R. Hegde, and J. Grant, "Fermi level pinning with sub-monolayer MeOx and metal gates," *IEEE Electron Device Meeting*, pp. 307-310, 2003.

[8] C. C. Hobbs, L. R. C. Fonseca, A. Knizhnik, V. Dhandapani, S. B. Samavedam, W. J. Taylor, J. M. Grant, L. G. Dip, D. H. Triyoso, R. I. Hegde, D. C. Gilmer, R. Garcia, D. Roan, M. L. Lovejoy, R. S. Rai, E. A. Hebert, H.-H. Tseng, S. G. H. Anderson, B. E. White, and P. J. Tobin, "Fermi-level pinning at the polysilicon/metal-oxide interface-Part II," *Electron Devices, IEEE Transactions on*, vol. 51, pp. 978-984, 2004.

[9] C. Hobbs, L. Fonseca, V. Dhandapani, S. Samavedam, B. Taylor, J. Grant, L. Dip, D. Triyoso, R. Hegde, D. Gilmer, R. Garcia, D. Roan, L. Lovejoy, R. Rai, L. Hebert, H. Tseng, B. White, and P. Tobin, "Fermi level pinning at the polySi/metal oxide interface," *VLSI Technology, 2003. Digest of Technical Papers. 2003 Symposium on*, pp. 9-10, 2003.

[10] C. Y. Wong, J. Y.-C. Sun, Y. Taur, C. S. Oh, R. Angelucci, and B. Davari, "Doping of n+ and p+ polysilicon in a dual-gate CMOS process," presented at Electron Devices Meeting, 2003. IEDM '03 Technical Digest. IEEE International, 1988.

[11] J. C. Hu, H. Yang, R. Kraft, A. L. P. Rotondaro, S. Hattangady, W. W. Lee, R. A. Chapman, C.-P. Chao, A. Chatterjee, M. Hanratty, M. Rodder, and I.-C. Chen,

"Feasibility of using W/TiN as metal gate for conventional 0.13 μm CMOS technology and beyond," *Electron Devices Meeting, 1997. Technical Digest., International*, pp. 825-828, 1997.

[12] ITRS, "ITRS Roadmap 2003," 2003.

[13] I. De, D. Johri, A. Srivastava, and C. M. Osburn, "Impact of gate work function on device performance at the 50 nm technology node," *Solid-State-Electronics*, vol. 44, pp. 1077-1080, 2000.

[14] E. H. Nicollian and J. R. Brews, *MOS Physics and Technology*. New york: Wiley, 1982.

[15] H. Michaelson, "The work function of the elements and its periodicity," *Journal of Applied Physics*, vol. 48, pp. 4729-4733, 1977.

[16] Y.-C. Yeo, T.-J. King, and C. Hu, "Metal-dielectric band alignment and its implications for metal gate complementary metal-oxide-semiconductor technology," *Journal of Applied Physics*, vol. 92, pp. 7266-7271, 2002.

[17] B.-Y. Tsui and C.-F. Huang, "Wide range work function modulation of binary alloys for MOSFET application," *IEEE Electron Device Letter*, vol. 24, pp. 153-155, 2003.

[18] M. A. Pawlak, T. Schram, K. Maex, and A. Vantomme, "Investigation of Iridium as a gate electrode for deep sub-micron CMOS technology," *Microelectronic Engineering*, vol. 70, pp. 373-376, 2003.

[19] B. Maiti and P. J. Tobin, "Metal Gates for Advanced CMOS Technology," *SPIE Conference on Microelectronic Device Technology III*, vol. 3881, pp. 46-57, 1999.

[20] H. Zhong, S. N. Hong, Y.-S. Suh, H. Lazar, G. Heuss, and V. Misra, "Properties of Ru-Ta alloys as gate electrodes for NMOS and PMOS silicon devices," *IEEE Electron Device Meeting*, 2001.

[21] I. Polishchuk, P. Ranade, T.-J. King, and C. Hu, "Dual work function metal gate CMOS transistors by Ni-Ti interdiffusion," *IEEE Electron Device Letter*, vol. 23, pp. 200-202, 2002.

[22] H. N. Alshareef, H. C. Wen, H. Luan, K. Choi, H. R. Harris, Y. Senzaki, P. Majhi, B. H. Lee, B. Foran, and G. Lian, "Temperature dependence of the work function of ruthenium-based gate electrodes," *Thin Solid Films*, vol. article in press Temperature dependence of the work function of ruthenium-based gate electrodes, 2006.

[23] R. Lin, Q. Lu, P. Ranade, T. J. King, and C. M. Hu, "An adjustable work function technology using Mo gate for CMOS devices," *Ieee Electron Device Letters*, vol. 23, pp. 49-51, 2002.

[24] S. H. Bae, W. P. Bai, H. C. Wen, S. Mathew, L. K. Bera, N. Balasubramanian, N. Yamada, M. F. Li, and D. L. Kwong, "Laminated metal gate electrode with tunable work function for advanced CMOS," presented at VLSI Technology, 2004. Digest of Technical Papers. 2004 Symposium on, 2004.

[25] G. Bersuker, P. Zeitzoff, J. H. Sim, B. H. Lee, R. Choi, G. Brown, and C. D. Young, "Mobility Evaluation in Transistors with Charge Trapping Gate Dielectrics," *Applied Physics Letters*, vol. 87, pp. 042905, 2005.

[26] H. N. Alshareef, H. C. Wen, H. R. Harris, K. Choi, H. F. Luan, P. Lysaght, P. Majhi, B. H. Lee, M. El-Bouanani, and V. Ukride, "Modulation of the work function of silicon gate electrode using thin TaN interlayers," *Applied Physics Letters*, vol. 87, 2005.

[27] S. Zafar, V. Narayanan, A. Callegari, F. R. McFeely, P. Jamison, E. Gusev, C. Cabral, and R. Jammy, "HfO/sub 2//metal stacks: determination of energy level diagram, work functions & their dependence on metal deposition," *VLSI Technology, 2005. Digest of Technical Papers. 2005 Symposium on*, pp. 44-45, 2005.

[28] C. C. Jr., C. Lavoie, A. S. Ozcan, R. S. Amos, V. Narayanan, E. P. Gusev, J. L. Jordam-Sweet, and J. M. E. Harper, "Evaluation of CMOS Gate Materials Using IN SITU Characterization Techniques," *Electrochemical Society Proceedings, Advanced Short-Time Thermal Processing for Si-Based CMOS Devices*, pp. 375-384, 2003.

[29] J. K. Schaeffer, S. B. Samavedam, D. C. Gilmer, V. Dhandapani, P. J. Tobin, J. Mogab, B. Y. Nguyen, B. E. White, S. Dakshina-Murthy, R. S. Rai, Z. X. Jiang, R. Martin, M. V. Raymond, M. Zavala, L. B. La, J. A. Smith, R. Garcia, D. Roan, M. Kottke, and R. B. Gregory, "Physical and electrical properties of metal gate electrodes on HfO2 gate dielectrics," *Journal of Vacuum Science & Technology B*, vol. 21, pp. 11-17, 2003.

[30] *CRC Handbook of Chemistry and Physics*, 70 ed. Boca Raton, Florida: CRC Press, Inc., 1989-1990.

[31] S. B. Samavedam, L. B. La, P. J. Tobin, B. White, C. Hobbs, L. R. C. Fonseca, A. A. Demkov, J. Schaeffer, E. Luckowski, A. Martinez, M. Raymond, D. Triyoso, D. Roan, V. Dhandapani, R. Garcia, S. G. H. Anderson, K. Moore, H. H. Tseng, C. Capasso, O. Adetutu, D. C. Gilmer, W. J. Taylor, R. Hegde, and J. Grant, "Fermi level pinning with sub-monolayer MeOx and metal gates [MOSFETs]," *Electron Devices Meeting, 2003. IEDM '03 Technical Digest. IEEE International*, pp. 13.1.1-13.1.4, 2003.

[32] J. Schaeffer, C. Capasso, L. R. C. Fonseca, S. Samavedam, L. B. La, J. Smith, S. Dakshina-Murthy, D. C. Gilmer, Luckowski, Y. Liang, S. Kalpat, B. Adetutu, H. H. Tseng, Y. Shiho, A. Demkov, R. Hegde, W. J. Taylor, R. Gregory, J. Jiang, E. Luckowski, M. Raymond, K. Moore, D. Triyoso, D. Roan, B. White, and P. J. Tobin, "Challenges for the integration of metal gate electrodes," *IEEE Electron Device Meeting*, 2004.

[33] K. Shiraishi, Y. Akasaka, S. Miyazaki, T. Nakayama, T. Nakaoka, G. Nakamura, K. Torii, H. Furutou, A. Ohta, P. Ahmet, K. Ohmori, H. Watanabe, T. Chikyo, M. L. Green, Y. Nara, and K. Yamada, "Universal theory of workfunctions at metal/Hf-based high-k dielectrics interfaces - guiding principles for gate metal selection," *Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International*, pp. 39-42, 2005.

[34] J. K. Schaeffer, L. R. C. Fonseca, S. B. Samavedam, Y. Liang, P. J. Tobin, and B. E. White, "Contributions to the effective work function of platinum on hafnium dioxide," *Applied Physics Letters*, vol. 85, pp. 1826-1828, 2004.

[35] E. Cartier, F. R. McFeely, V. Narayanan, P. Jamison, B. P. Linder, M. Copel, V. K. Paruchuri, V. S. Basker, R. Haight, D. Lim, R. Carruthers, T. Shaw, M. Steen, J. Sleight, J. Rubino, H. Deligianni, S. Guha, R. Jammy, and G. Shahidi, "Role of oxygen vacancies in V/sub FB//V/sub t/ stability of pFET metals on HfO/sub 2/," *VLSI Technology, 2005. Digest of Technical Papers. 2005 Symposium on*, pp. 230-231, 2005.

[36] D. Gu, S. K. Dey, and P. Majhi, "Effective work function of Pt, Pd, and Re on atomic layer deposited HfO[sub 2]," *Applied Physics Letters*, vol. 89, pp. 082907, 2006.

[37] H. Yang, Y. Son, S. Baek, H. Hwang, H. Lim, and H.-S. Jung, "Ti gate compatible with atomic-layer-deposited HfO[sub 2] for n-type metal-oxide-semiconductor devices," *Applied Physics Letters*, vol. 86, pp. 092107, 2005.

[38] R. Chau, S. Datta, M. Doczy, B. Doyle, J. Kavalieros, and M. Metz, "High-k/Metal–Gate Stack and Its MOSFET Characteristics," *IEEE Electron Device Letter*, vol. 25, pp. 408-410, 2004.

[39] A. C. V. Narayanan, F.R. McFeely, K. Nakamura, P. Jamison, S. Zafar, E. Cartier, A. Steegen, V. Ku, P. Nguyen, K. Milkove, C. Cabral Jr., M. Gribelyuk, C. Wajda, Y. Kawano, D. Lacey, Y. Li, E. Sikorski, E. Duch, H. Ng, C. Wann, R. Jammy, M. Ieong, G. Shahidi, "Dual Work Function Metal Gate CMOS using CVD metal electrodes," *VLSI Technology Digest*, pp. 192-193, 2004.

[40] C. Young, G. Bersuker, H. C. Wen, G. Brown, and P. Majhi, "Charge Trapping Characteristics of Hafnium Based High-ê Dielectrics with Various Metal Electrodes," *SSDM 2004*, 2004.

[41] P. Majhi, C. Young, G. Bersuker, H. C. Wen, G. A. Brown, B. Foran, R. Choi, P. M. Zeitzoff, and H. R. Huff, "Influence of Metal Gate Materials and Processing on Planar CMOS Device Characteristics with High-k Gate Dielectrics," *ESSDERC*, 2004.

[42] http://www.intel.com/technology/mooreslaw/index.htm, "Moore's Law Means More Performance."

CHAPTER 2

STANDARDIZED EFFECTIVE WORK FUNCTION EXTRACTION TECHNIQUE: TERRACED OXIDE

2.1 MOTIVATION

The traditional method for EWF extraction on SiO_2 dielectrics is through C-V measurement of the flatband voltage (V_{fb}) for a thickness series of the dielectric, and extracted linearly by the V_{fb}-EOT relationship (Figure 1.4)[1]. However, when varying high-k dielectric thicknesses, bulk charges in the dielectric (ρ_b) shift the $V_{fb.}$ The interfacial SiO_x layer between the high-k and the Si substrate also varies with high-k thickness and makes it difficult to maintain a constant fixed interface charge at the Si-dielectric interface (Q_f). Figure 2.1 is the schematic showing various charges in stack which contribute to V_{fb}. EWF extraction is no longer easily extracted from a linear relationship, but a complex quadratic formula (Equation 2-1). [2]

$$V_{fb} = \Phi'_{ms} - \frac{Q_f * EOT}{\varepsilon_{ox}} - \left(\frac{Q_i * t_h}{\varepsilon_h} - \frac{1}{\varepsilon_h}\int_0^{t_h} x\rho_b(x)dx - \frac{1}{\varepsilon_{ox}}\int_{t_h}^{t=t_h+t_o} x\rho_{ox}(x)dx\right) \quad \text{....Equation 2-1}$$

Without fully calculating the charge contributions, many still report EWF values using a linear extraction, resulting in large errors due to inaccurate fitting. Examples of the quadratic dependence of V_{fb}-EOT plot, and its deviation by using linear fitting is shown in Figure 2..2, especially if the high-k quality is poor and exhibits large bulk charges. The inaccuracy in the EWF extraction could be accounted for the disparity in the various reported EWFs of a given material system (Figure1-8) [3], and thus complicates the study of metal gate EWF, and the progression to achieving band edge EWF materials. Therefore, an accurate EWF extraction technique is critical as the foundation of metal gate work.

2.2 EXPERIMENTAL PROCEDURES OF THE TERRACED OXIDE TECHNIQUE

On a single device wafer with field isolation, the dielectric is thermally grown SiO_2 (10nm) and etched into ringed-terraces of various thicknesses with a benign wet etching of diluted hydrofluoric acid. The SEZ^{TM} Model 203 spin etch processor was used for the fabrication of our terraced oxides. Standard terraced oxide thicknesses of 2, 4, 6, 8nm (thick terraces) or 0, 2, 3, 4nm (ultra-thin terraces) are typically used. Details of this process can be found in [4]. The quality of the terrace oxides is found to be comparable to that of as grown thin oxides. Figure 2.3 is a photo of a blanket terraced oxide wafer with thick oxides for enhanced color contrast and a schematic of terraced oxide devices . For EWF extraction on high-k, the deposition of a thin high-k film (2~3nm) is added to the terraced oxide wafers, then followed by metal electrode deposition. A tungsten (W) or poly-Si capping layer is then deposited for ease of device testing, or to prevent metal oxidation during subsequent thermal budgets. Capacitor devices were formed and EWF was measured after a low temperature forming gas anneal, or after a 1000^{o}C, 5 sec activation anneal required to activate the dopants in CMOS device processes. C-V curves were measured at 100 kHz using an Agilent 4284A measurement system, and the V_{fb} and EOT values were computed from the NCSU CVC program [5].

2.2.1 Charge model of the terraced oxide technique

The terraced oxide method follows a three charge model to enable linear V_{fb}-EOT extraction [6, 7] (Equation 2-3). The equation is a simplified form of the general model given by R. Jha [2] (or Equation 2-2) and thus enable linear extraction of the V_{fb}-EOT relationship by use of good quality terraced oxides, and limiting the SiO_2 contribution (ρ_{ox}) to the equation:

$$V_{fb} = (\Phi'_{ms} - \frac{Q_i * EOTh}{\varepsilon_{ox}} - \frac{\rho_b * (\varepsilon_h / \varepsilon_{ox}) * EOTh^2}{2 * \varepsilon_{ox}}) - \frac{Q_f * EOT}{\varepsilon_{ox}}; \quad t_h = \frac{\varepsilon_h}{\varepsilon_{ox}} EOTh$$ ..Equation 2-3

With the use of terraced oxide structures, a constant fixed interface charge between the Si substrate and dielectric (Q_f) is maintained across the varying oxide thicknesses, minimizing wafer-to-wafer variation associated with multiple wafer extraction methods. Q_f can be calculated from the slope of the V_{fb}-EOT relationship. The SiO_2 bulk charge term in reference [2] (ρ_{ox}) can be neglected for simplification of the extraction since this bulk charge contribution is far smaller than that of Q_f.[8] The extracted y-axis ordinate intercept value contains the contribution of the metal WF as well as the high-k/SiO_2 interface charge (Q_i) and high-k bulk charge density (ρ_b) terms. (t_h: high-k physical thickness, EOT_h: high-k EOT; EOT: EOT of high-k/SiO_2 stack, ε_h: high-k dielectric constant, ε_{ox}: SiO_2 dielectric constant).

The contributions of charges in the high-k on V_{fb} is controlled and can be minimized (~+50 meV), by using a fixed and thinned high-k film (2~3nm). More on the calculations for the bulk charge contribution will be discussed in the next section. Therefore, for simplicity, the ordinate intercept value is the EWF values quoted when extracting with the terraced oxide method.

2.3 DEMONSTRATION OF THE TERRACED OXIDE EXTRACTION

A comparison of V_{fb}-EOT plots for metal/$HfSiO_x$ gate stacks using a single terraced oxide-fixed-thickness high-k wafer (linear extraction) and multiple oxide-variable-thickness-high-k wafers (quadratic extraction) illustrates the advantage of the terraced oxide stack approach (Figure 2.4) for reduce errors in extraction. More examples of the application of the terraced oxide technique for EWF extraction is shown through this work and has proven to be extremely sensitive to slight changes in metal EWF.

2.3.1 Using the terraced oxide method for calculation of high-κ stack charges

To obtain the contribution of high-k bulk charge and high-k/oxide interface charge terms, an experiment was designed with multiple terraced oxide wafers identical except for varying constant high-k thickness (5cy, 15cy, 25cy, 30Å, 35Å, 45Å, 65Å ALD HfO_2 and $HfSiO_x$). Their V_{fb}-EOT y-intercept values (Φ_i) are plotted versus the high-k EOT values, and the Φ_i versus EOT_h relationship should follow Equation 2-4. In Figure 2.5 Φ_i is plotted versus the physical thickness, in terms of ALD deposition cycles.

$$\Phi i = \Phi'_{ms} - \frac{Q_i * EOT_h}{\varepsilon_{ox}} - \frac{\rho_b * (\varepsilon_h / \varepsilon_{ox}) * EOT_h^2}{2 * \varepsilon_{ox}} \quad \text{....Equation 2-4}$$

A linear plot implies a constant Q_i and negligible ρ_b. The SiO_2-high-k interface charge density, Q_i, may be computed from the slope of the plot. For ALD TiN gate electrodes on both HfO_2 and $HfSiO_x$, a linear relationship is observed, and similar Q_i/q is calculated to be ~$1.6x10^{12}/cm^2$. A non-linear plot may imply the presence of bulk charge ρ_b in the high-k film or the combination of Q_i and ρ_b. With sufficient data it may be possible to solve for both Q_i and ρ_b. The ordinate y-axis intercept of this Φ_i–EOT_h plot is the gate electrode-substrate work function difference for the high-k stack system (At EOT_h=0, Φ_{ms}=-0.47eV on $HfSiO_x$, and -0.53 on HfO_2; correlats to a work function of ~4.6eV, and 4.54eV, similar to the work function of ALD TiN on SiO_2 in this experiment: 4.54eV. This result suggest there is no reaction between the TiN and high-k films, which will otherwise result in difference in effective work function.

The terraced oxide approach is therefore useful for evaluating work function of metal electrodes on high-k films if the fixed high-k deposited is thin enough to limit the effect of the interface charge term (which is proportional to EOT_h). Using standard 20Å or 30Å $HfSiO_x$ and HfO_2, maximum deviation of the ordinate intercept value extracted

from the V_{fb}-EOT plot is found to be 50~100meV from the actual effective work function of metal on high-k. Therefore, for simplicity, the ordinate intercept value is the EWF values quoted when extracting with the terraced oxide method.

2.4 VALIDATION OF TERRACED OXIDE EWF EXTRACTION: COMPARISON WITH CURRENT EXTRACTED BARRIER HEIGHT

The V_{fb} is not only impacted by charge, but also is influenced by the presence of other factors. Therefore, EWFs for metal gate electrodes on high-k dielectrics extracted from the V_{fb} can be a combination of the true metal WF + dielectric stack charges + interface dipole formation [9]. However, the actual work function (WF) with respect to vacuum can be calculated by measuring the metal/dielectric barrier height (Φ_b) once the electron affinity of a dielectric is known. Extracting Φ_b by monitoring the gate current density- gate voltage- temperature (J_g-V_g-T) relationship (V_g>0) for MOS devices has been reported by Zafar et al. [10-12]. Accuracy of the terraced oxide (C-V based) method can be confirmed via comparison with the metal/high-k barrier height. We will cross compare the C-V extracted EWF with that estimated from barrier height measurements.

2.4.1 The current extracted barrier height (J-V) method

If the main conduction mechanism is tunneling, the voltage applied when the conduction mechanism transitions from direct tunneling to Fowler-Nordheim (F-N) tunneling corresponds to the Φ_b at the metal/dielectric interface (Figure 2.6). This technique provides a direct measurement of the metal/dielectric barrier height without the impact of fixed oxide charges, nor knowledge of oxide fields. Restriction of this method is the ability to measure the tunneling current without the dielectric undergoing early breakdowns, which may be the case for ultra thin SiO_2 layers.

2.4.2 Sample requirements and preparation for J-V barrier height method

The same terraced oxide structures for EWF extraction via C-V measurements can be used for J-V if the samples are properly prepared. Highly doped n-type Si substrates (N_d=1E18/cm^3) are preferred as starting substrates to limit additional voltage drop in the Si substrate at accumulation for the J-V barrier height extraction. A thin terraced oxide is used with SiO_2 thicknesses of 1.0, 1.5, 2.5, 3.5nm, followed by atomic layer deposition of 3nm of HfO_2 film and various metal gate electrodes, and a tungsten or poly-Si capping layer. Film thicknesses are critical in order to see the transition point for current conduction. Capacitor devices were formed and EWF was measured after a low temperature forming gas anneal, or after a 1000^{o}C, 5 sec activation anneal. J-V measurements were made with a staircase voltage sweep with step size = 0.025V, and on small area capacitors (area = 3e-6/cm^2) to minimize defect-enhanced leakage currents.

2.4.3 Comparison of terraced oxide (C-V) vs barrier height (J-V) techniques

V_{fb}-EOT plots for EWF extraction on terraced oxide (SiO_2) and terraced oxide + high-k (HfO_2) are shown in Figure 2.7(a)(b). The extracted EWF for TiN/SiO_2 is 4.62eV, with a fixed charge $Q_{f=}$-6E11/cm^2. The V_{fb}-EOT for TiN/HfO_2 exhibits an excellent linear relationship, suggesting minimum influence of ρ_b, with EWF=4.66eV and Q_f=2E11/cm^2. Well behaved C-Vs for corresponding to the varied EOT devices across the terraces are shown in the insert of both samples.

Leakage current measurements were performed on the same terraced oxide capacitor structures. The band diagram for metal/SiO_2 and metal/high-k/SiO_2 MOS devices in accumulation corresponding to the onset of current mechanism change (at $V_{g\ peak}$= Φ_b) is shown in Figure 2.6. For SiO_2 (Figure 2.6(a)), the barrier height is the applied voltage at the maximum of the Δln(J)/ ΔV curve (the ΔJ_V method in [10]). With 3

nm HfO_2 on 2~3nm SiO_2 stacks, current across the SiO_2 is completely in the direct tunneling regime, and the peak of the $\delta\ln(J)/\delta V$ curve corresponds to the onset of Fowler-Nordheim (F-N) tunneling in the high-k film, as shown in the band diagram schematic in Figure 2.6(b). ΔJ_V results for both stacks are shown in Figure 2.8(a). The various $\Delta\ln(J)/\Delta V$ curves represent current measurements across the radius of the wafer, reflecting variations in EOT on the terraced oxide wafer. TiN/SiO_2 barrier height (Φ_{bo}), is at V_{gpeak}=~3.7+/- 0.05V. This transforms to a TiN metal work function of 4.6+/- 0.05V with the addition of the SiO_2 electron affinity χ=0.9, consistent with that extracted from the terraced oxide technique. Also worthy of note is that the peak intensity is most evident for SiO_2 thicknesses of the range 2.7~3.5nm, corresponding to the transition point from direct to F-N tunneling at electric fields 8~9MV/cm [13]. The measured TiN/HfO_2 barrier height (Φ_{bh}) is at V_{gpeak}~2.00+/- 0.05V. Since the metal work functions on high-k and SiO_2 are equal, as obtained from the terraced oxide results in this study, the conduction band offset (ΔEc) between HfO_2 and SiO_2 can be calculated to be Φ_{bo}-Φ_{bh}= 1.7eV. This value is slightly different from that (2eV) reported by Zafar in [12]. Modeling the band offset for oxides was previously reported by Robertson, and Demkov [14, 15]. The calculated ΔEc is a function of the charge neutrality levels (CNL) of HfO_2 and its electron affinity, which may depend on the high-k processing conditions since film structure (ex. monoclinic-HfO_2 versus tetragonal structures) will influence the CNL. Nevertheless, for mono-clinic HfO_2, the ΔE_c measured (1.7eV) should reside within the Schottky and Bardeen limits of the calculations, which is estimated to be between 1.6~2eV, respectively [15]. ΔJ_V for the HfO_2/SiO_2 sample has also been conducted at temperatures ranging from 250-100^oK to limit influence of thermal emission currents (Figure 2.8 (b)). A shift in the ΔJ_V peak to a higher voltage ~80meV at 100^oK is observed which may be attributed to a similar amount of shift in the Fermi-level at 100^oK [16],

thus validating the measured Φ_{bh} even at low temperatures. The ΔJ_T method as described by Zafar in [10], ($\Delta J_T=[J(T_1)-J(T_2)]/J(T_2)$) will also have a maximum when $V_{gpeak}= \Phi_b$. ΔJ_T for 300 and 100^{o}K is shown in (Figure 2.8(b)) ; it has been found to align well with that for the ΔJ_V measurements.

A comparison of the EWF extracted by the terraced oxide technique on high-k films, and WF calculated from the barrier height (measured with ΔE_c~1.7eV) is shown in Figure 2.9 for multiple metal/high-k devices with maximum process thermal budget of 1000^{o}C. A reasonable correlation is consistently obtained for various metal gate materials with EWF deviations of +/-0.1V. The metal gates materials used in this study contained pure metals, nitrides, and silicides, which exhibit good thermal stability with the dielectric [17]. Consequently, interfacial reactions of metals with high-k or SiO_2 that may change the EWF is negligible.

2.5 CONCLUSIONS

The terraced oxide technique is proposed to be an accurate EWF extraction technique allowing linear extraction of the V_{fb}-EOT relationship. The EWF for metal/high-k stacks calculated using the ordinate intercept value may be impacted by 1) dielectric bulk charges or 2) other factors such as formation of metal/high-k dipole. Calculations of dielectric charges suggest use of thin high-k enables control of charge contributions to EWF to ~50-100meV. Comparisons of the EWF extracted by the terraced oxide technique with the barrier height calculated WF by the J-V measurements have exhibited a reasonable correlation, suggesting real change in metal work function is being measured, validating both techniques for EWF extraction [4].

Combining the terraced oxide method, which gives the EWF, and the J-V method, which provides a true WF by metal/dielectric barrier height measurement, will allow

quantification and enhance learning on the other factors that have been reported to influence the EWF for metal gate electrodes and are not well understood.

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2.6 FIGURES

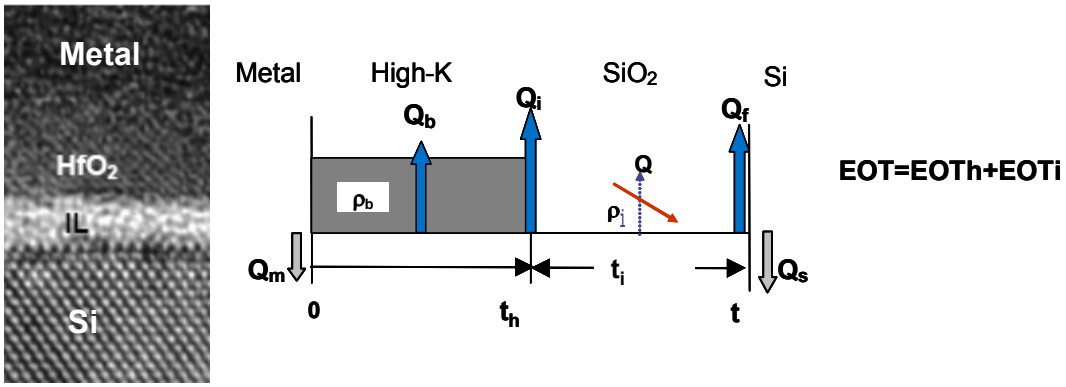


Figure 2.1 High resolution transmission electron image of dielectric stacks, and the corresponding charge terms within the stack. (Q_m: charge at the electrode/high-k interface; Q_b: effective bulk charge in the high-k dielectric with centroid at center of high-k derived from bulk charge density (ρ_b); Q_i: interface charge between high-k and SiO_2; Q: effective bulk charge in SiO_2 region due to bulk charge (ρ_{ox}); Q_f: fixed charge at the Si/SiO_2 interface) (t: total thickness of the film; t_h: physical thickness of the high-k; t_i: thickness of the interface SiO_2)

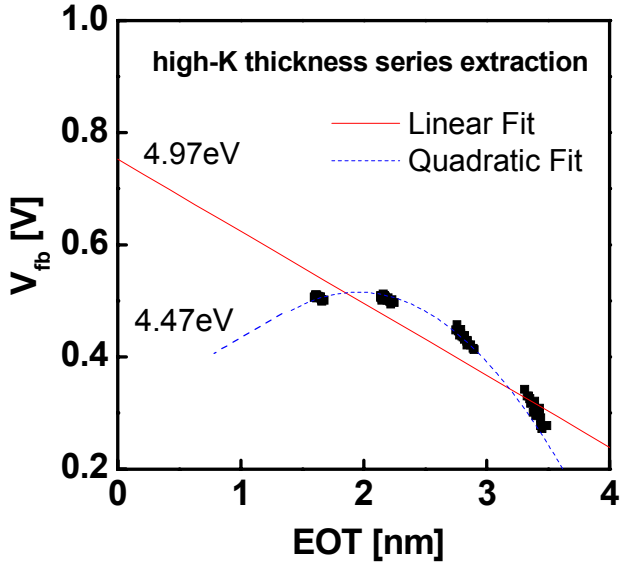


Figure 2.2 Comparison of the V_{fb}-EOT plot for EWF extraction using linear extraction on multiple high-k thickness series wafers.

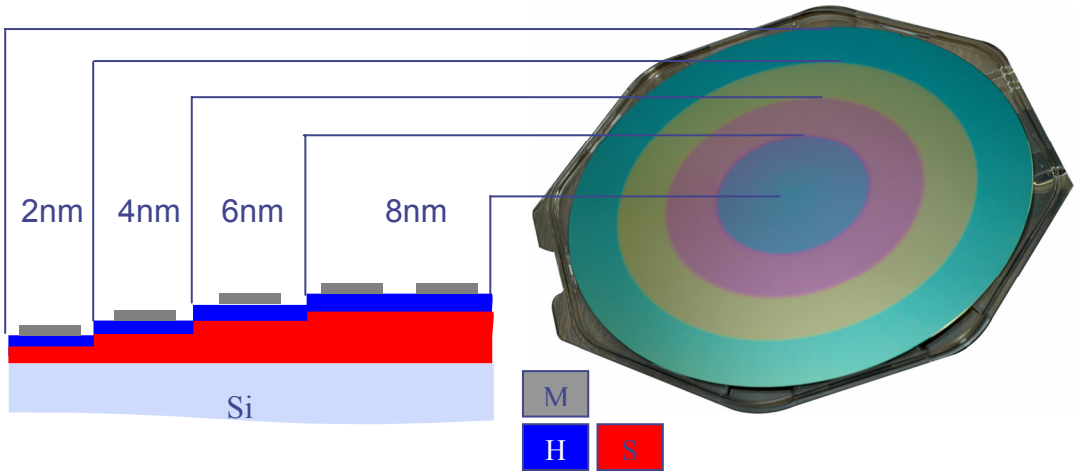


Figure 2.3 Photo of terraced oxide wafers with enhanced color contrast of SiO_2 thickness bands and the corresponding schematic of devices formed on terraced oxide wafers. (M: metal; H: high-k; S: SiO_2)

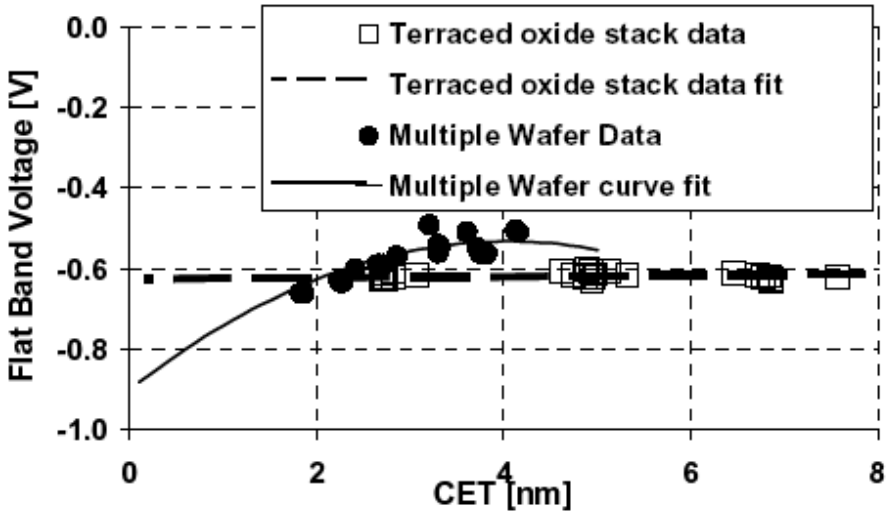


Figure 2.4 Comparison of EWF extraction from terraced oxide stack results versus from multiple wafers with high-k dielectric thickness series.

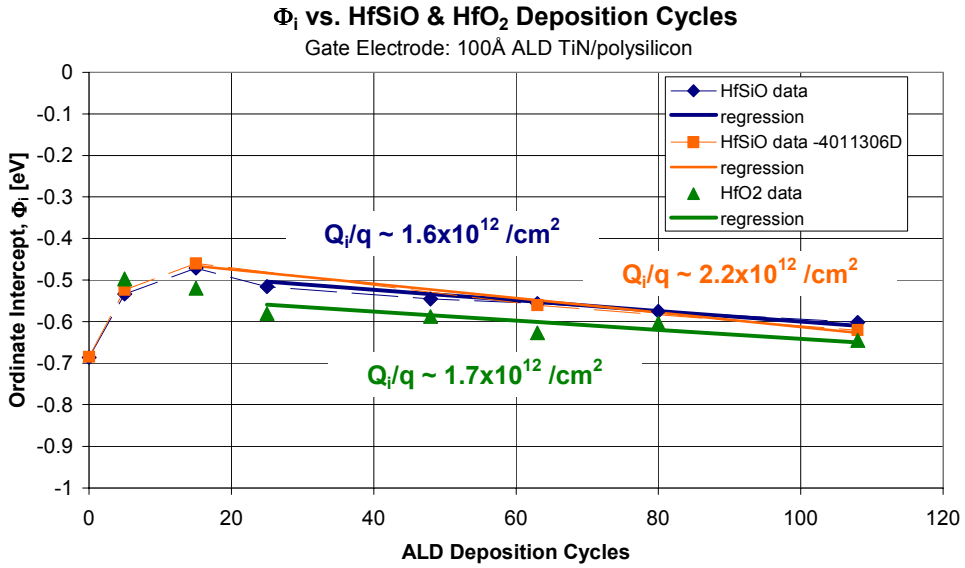


Figure 2.5 **Ordinate intercept versus high-k thickness(deposition cycles), slope of this relationship is the SiO_2/high-k interface charge Q_i.**

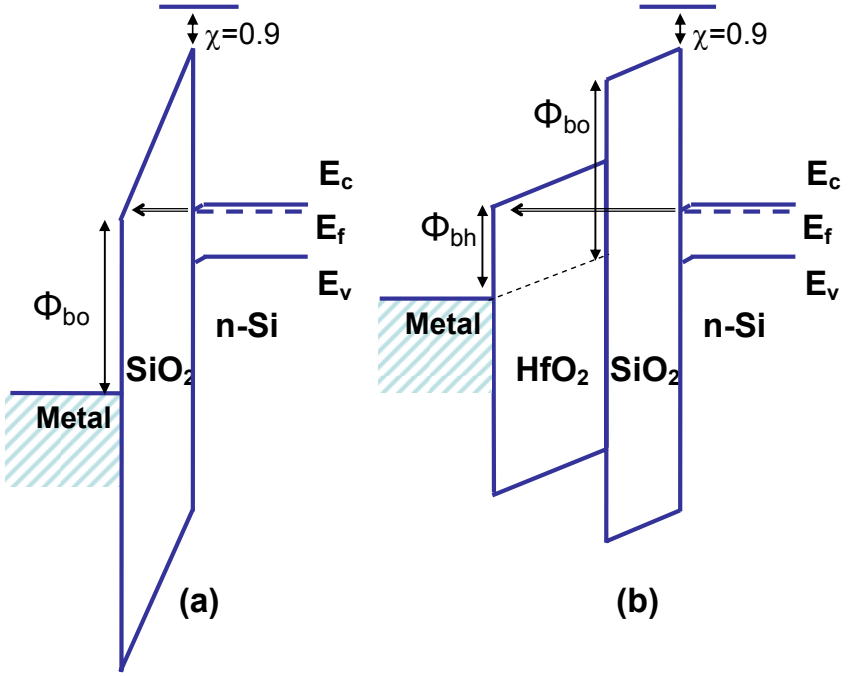


Figure 2.6 **Schematic band diagram of the (a) metal/SiO_2/n-Si, and (b) metal/HfO_2/SiO_2/n-Si stack in accumulation at onset of direct to F-N tunneling.**

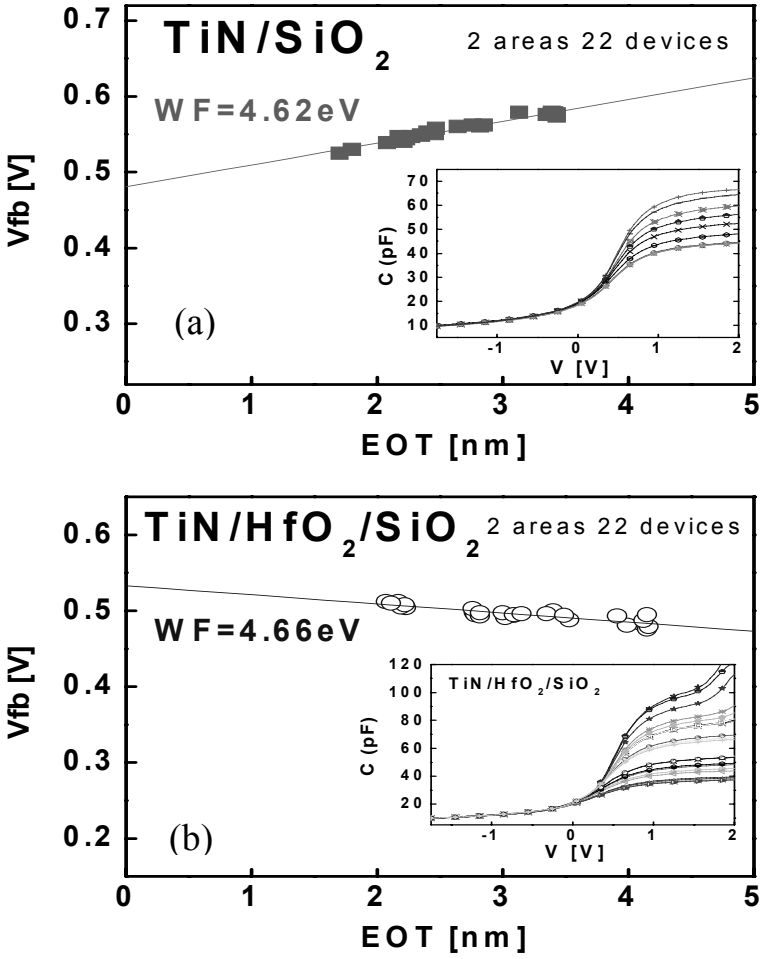


Figure 2.7 **V_{fb}-EOT plot for EWF extraction of (a) TiN/SiO_2 and (b) $TiN/HfO_2/SiO_2$ stacks from terraced oxide structures. C-Vs for corresponding to the varied EOT devices across the terraces are shown in the insert.**

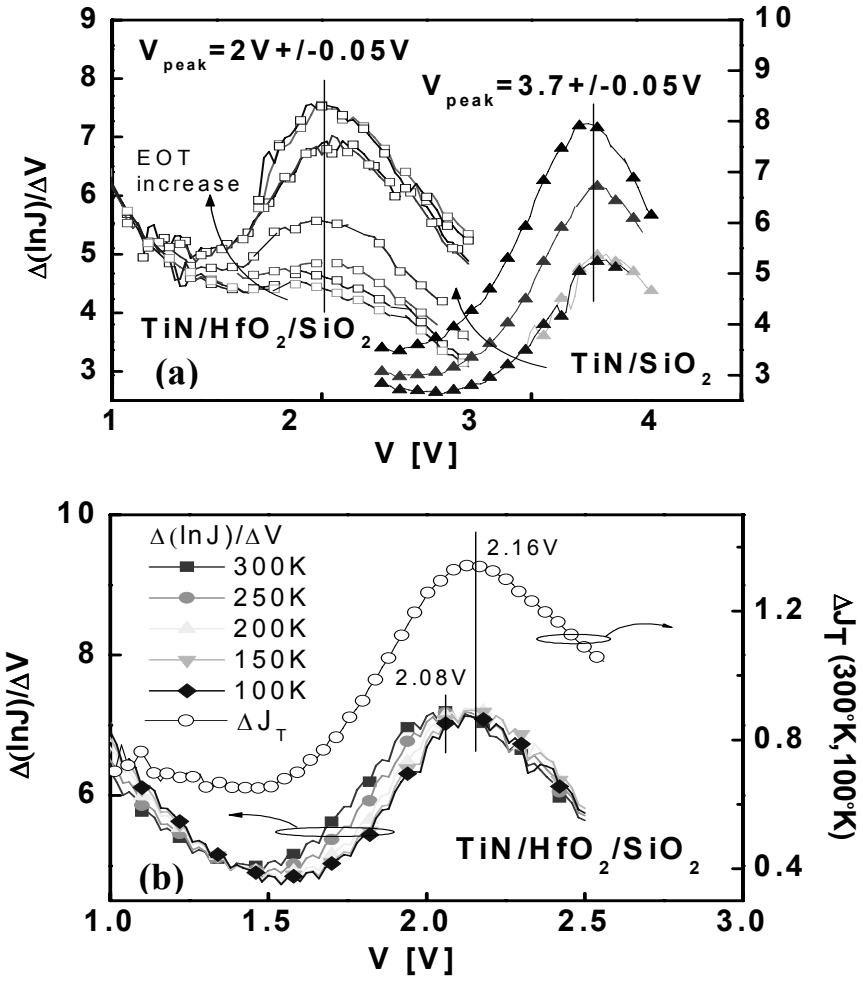


Figure 2.8 (a) Δ(lnJ)/ ΔV versus V plots from J-V curves of TiN/SiO_2 and $TiN/HfO_2/SiO_2$ stacks measured on the terraced oxide structures. (b) ΔJ_V and ΔJ_T for $TiN/HfO_2/SiO_2$ stacks measured at 300-100°K.

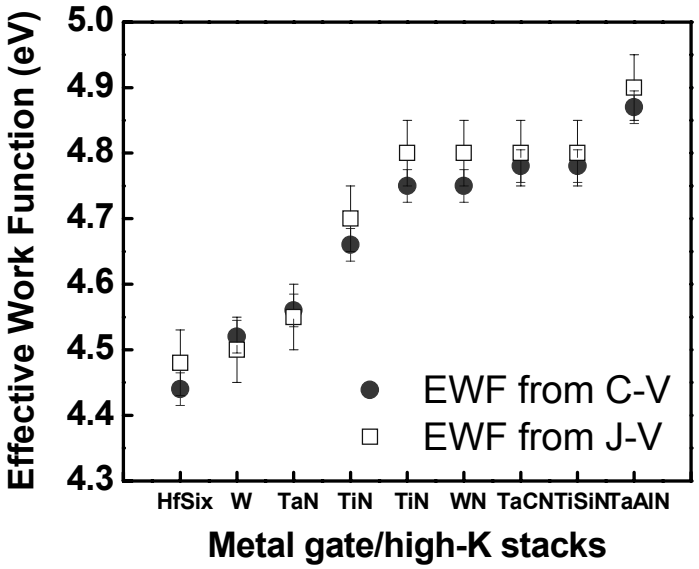


Figure 2.9 Comparison of the EWF of various metal gate electrodes extracted from terraced oxide/high-k stack structures with calculated WF from barrier height extraction (with ΔE_c=1.7eV).

2.7 REFERENCES

[1] D. V. Lang, *Thermally Stimulated Relaxation in Solids*, vol. 37. Berlin: Springer, 1979.

[2] R. Jha, J. Gurganos, Y. H. Kim, R. Choi, J. Lee, and V. Misra, "A capacitance-based methodology for work function extraction for metals on high-k," *IEEE Electron Device Letter*, vol. 25, pp. 420-423, 2004.

[3] P. Majhi, H. C. Wen, H. Alshareef, K. Choi, R. Harris, P. Lysaght, H. Luan, Y. Senzaki, S. C. Song, B. H. Lee, and C. Ramiller, "Evaluation and integration of metal gate electrodes for future generation dual metal CMOS," *Integrated Circuit Design and Technology, 2005. ICICDT 2005. 2005 International Conference on*, pp. 69-72, 2005.

[4] H. C. Wen, R. N. Choi, G. A. Brown, T. Boscke, K. Matthews, H. R. Harris, K. Choi, H. N. Alshareef, H. F. Luan, G. Bersuker, P. Majhi, D. L. Kwong, and B. H. Lee, "Comparison of effective work function extraction methods using capacitance and current measurement techniques," *Ieee Electron Device Letters*, vol. 27, pp. 598-601, 2006.

[5] J. R. Hauser and K. Ahmed, "Characterization of Ultra-Thin Oxides Using Electrical C-V and I-V Measurements," *Characterization and Metrology for ULSI Technology: 1998 International Conference*, vol. 449, pp. 235-239, 1998.

[6] G. Brown, G. Smith, J. Saulters, K. Matthews, H. C. Wen, P. Majhi, and B. H. Lee, "An Improved Methodology for Gate Electrode Work Function Extraction in SiO2 and High-k Gate Stack Systems Using Terraced Oxide Structures," *IEEE SISC conference*, 2004.

[7] H. N. Alshareef, Z. Zhang, P. Majhi, G. Brown, P. Zeitzoff, H. Huff, and B. H. Lee, "Gate electrode development for dual metal-gate CMOS applications," in *Future Fab*, vol. 19, 2005, pp. 91-93.

[8] G. D. Wilk, M. L. Green, M.-Y. Ho, B. W. Busch, T. W. Sorsch, F. P. Klemens, B. Brijs, R. B. van Dover, A. Kornblit, T. Gustafsson, E. Garfunkel, S. Hillenius, D. Monroe, P. Kalavade, and J. M. Hergenrother, "Improved film growth and flatband voltage control of ALD HfO/sub 2/ and Hf-Al-O with n/sup +/ poly-Si gates using chemical oxides and optimized post-annealing," presented at VLSI Technology, 2002. Digest of Technical Papers. 2002 Symposium on, 2002.

[9] C. C. Hobbs, L. .Fonseca, A. Knizhnik, V. Dhandapani, S. B. Samavedam, W. J. Taylor, J. M. Grant, L. G. Dip, D. H. Triyoso, R. I. Hegde, D. C. Gilmer, R. Garcia, D. Roan, M. L. Lovejoy, R. S. Rai, E. A. Hebert, H.-H. Tseng, S. G. H. Anderson, B. E. White, and P. J. Tobin, "Fermi-Level Pinning at the Polysilicon/Metal–Oxide Interface—Part II," *IEEE Transactions on Electron Devices*, vol. 51, pp. 978-984, 2004.

[10] S. Zafar, C. Cabral, A. R., and A. Callegari, "A method for measuring barrier heights, metal work functions and fixed charge densities in metal/SiO2/Si capacitors," *Applied Physics Letters*, vol. 80, pp. 4858-4860, 2002.

[11] S. Zafar, E. Cartier, and E. P. Gusev, "Measurement of barrier heights in high permittivity gate dielectric films," *Applied Physics Letters*, vol. 80, pp. 2749-2751, 2002.

[12] S. Zafar, V. Narayanan, A. Callegari, F. R. McFeely, P. Jamison, E. Gusev, C. Cabral, and R. Jammy, "HfO/sub 2//metal stacks: determination of energy level diagram, work functions & their dependence on metal deposition," *VLSI Technology, 2005. Digest of Technical Papers. 2005 Symposium on*, pp. 44-45, 2005.

[13] T. Hori, *Gate Dielectrics and MOS ULSI Principles, Technologies and Application*: Springer-Verlag Berlin Heidelberg, 1997.

[14] J. Robertson, "Band offsets of wide-band-gap oxides and implications for future electronic devices," presented at Papers from the international conference on silicon dielectric interfaces, 2000.

[15] A. A. Demkov, L. R. C. Fonseca, E. Verret, J. Tomfohr, and O. F. Sankey, "Complex band structure and the band alignment problem at the Si--high-k dielectric interface," *Physical Review B (Condensed Matter and Materials Physics)*, vol. 71, pp. 195306, 2005.

[16] A. S. Grove, *Physics and Technology of Semiconductor Devices*. New York: Wiley, 1967.

[17] P. Majhi, H.-C. Wen, K. Choi, H. Alshareef, C. Huffman, and B. H. Lee, "A systematic study of the influence of nitrogen in tuning the effective work function of nitrided metal gates," presented at VLSI Technology, 2005. (VLSI-TSA-Tech). 2005 IEEE VLSI-TSA International Symposium on, 2005.

CHAPTER 3

DECOUPLING THE FERMI LEVEL PINNING EFFECT IN METAL GATE AND HIGH-κ STACK

3.1 MOTIVATION

The Fermi-level (E_f) pinning effect between metal/high-k, had widely been used to explain why the effective work function (EWF) of metal electrodes on high-k would be different from its bulk value, and on SiO_2 [1-3] The metal induced gap states (MIGS) model explains the E_f will pin toward the charge neutrality level in the high-k and become an intrinsic limitation for obtaining band edge EWF metal electrodes on high-k dielectrics [4, 5]. Many literature reports suggest the experimental EWF results agree with the MIGS predictions [1, 6], however, recently detailed studies of many of these electrode systems suggest contributions from extrinsic factors. Extrinsic contributions include: defect states induced by the electrode (oxygen vacancy model)[7-9], chemical reduction of the high-k interface [10], or material characteristic changes in the electrode [11, 12]. Dr. Shiraishi has proposed a grand theory for metal EWF based on a combination of the MIGS concept (intrinsic) as well as the O vacancy contributions (extrinsic), where the charge neutrality level changes depending on the metal system [13]. The result of such extrinsic factors should be acknowledged as E_f deviation, and not "pinning" since E_f is no longer pinned to an intrinsic value, however the term E_f-pinning is loosely used for stacks with different EWF on high-k. The advances in this field now questions whether experimental results correlate to the initial MIGS model after separating out extrinsic contributions, and whether an intrinsic limitation does exist for EWF tuning on high-k.

To enable study of the real intrinsic contribution in EWF on high-k, systematic studies in understanding true factors contributing to EWF on high-k dielectrics, as well as separation of extrinsic effects (such as interfacial reaction, interdiffusion, especially the role of interfaces, etc.) is needed. Since any deviation of EWF on high-k from SiO_2 maybe perceived as E_f-pinning effects, inaccurate determination of EWF may induce complications in the observations. Thus through accurate EWF extraction by the terraced oxide method, comparison with the MIGS intrinsic model is performed to address the intrinsic contributions of E_f-pinning.

3.2 MODELS ON INTRINSIC FACTORS OF EWF CONTROL

3.2.1 MIGS model for E_f-pinning

The metal induced gap states (MIGS) model has been proposed to be the intrinsic component inducing E_f-pinning [4, 5]. The MIGS model suggests due to the presence of intrinsic interface states, as the electrode is in contact with a dielectric, interfacial charge exchange will occur causing the metal E_f to shift toward a characteristic energy level in dielectric, the charge neutrality level (Φ_{CNL}) (Figure 3.1). The Φ_{CNL} is the location of the highest occupied surface state in the dielectric band gap. The degree of the metal E_f level shift depends on the pinning strength of the dielectric, the Schottky pinning parameter S, and thus the EWF ($\Phi_{m,eff}$) is related to its vacuum work function (Φ_m) with the relationship:

$$\Phi_{m,eff} = \Phi_{CNL} + S(\Phi_{m,vacc} - \Phi_{CNL})$$

The S parameter is dependent on the electronic component of the dielectric constant ε_∞ dielectric characteristic and follows the equation:

$$S = \frac{1}{1 + 0.1(\varepsilon_\infty - 1)^2}$$

This suggests dielectrics with higher dielectric constants will have greater degree of pinning, and will especially limit the choices of obtaining band edge EWF on high-k dielectrics.

3.2.2 Experimental results in literature

Experimental EWF results in the literature have shown reasonable correlation (Figure 3.2) [3, 4] with the MIGS prediction, and empirically calculated the Φ_{CNL} of HfO_2 to be ~4.4eV. However, other results still exhibit a reasonable degree of EWF span for Ti and Pt electrodes [13, 14]. Further investigation has shown electrodes with high WF such as Pt, Re and Ru, exhibit much lower EWF on high-k [7-9, 11]. Comparison of the EWF reduction for Pt versus the MIGS model prediction give a pinning factor S=0.15, or 0.25 much higher than the intrinsic limitation of S=0.53 for HfO_2 [8], possibly due to extrinsic effects. Whether an accurate EWF extraction was performed will also complicate the learning. Therefore, results in the literature may not be completely explained by MIGS, and require careful analysis.

3.3 SEPARATION OF EXTRINSIC CONTRIBUTIONS

3.3.1 Interface chemical reaction, materialistic change in the electrode

A material system often used as an example of E_f-pinning on high-k is the Ru metal, where on SiO_2 high EWF is observed (5eV), while low WF is obtained on high-k (4.6eV) (Figure 3.3(a)). Through a systematic analysis of the reaction mechanism at the Ru dielectric interface [15], we find that Ru easily reacts with SiO_2 and is more thermally stable on Hf-based high-k. The formation of a RuO_x like interface at the Ru/SiO_2 interface is the source of the high EWF, since RuO_2 is a high vacuum WF material. The reaction is easily observed at elevated temperatures through a high resolution TEM

image, shown in Figure 3.4(b)[12]. Cross comparison of EWF results with intentional RuO_x deposition on high-k also reproduces the high 5eV EWF. This observation is consistent with that reported by Panstiano et al. [11]; when annealing Ru in an oxidizing environment, a higher EWF is shown on both high-k and SiO_2. This suggests the modification induced at the metal/dielectric interface is due to materialistic changes, like oxidation in the electrode, and not dominated by E_f-pinning like effects..

Another more subtle interface chemical reaction is reported for high WF Pt and Re electrodes (5.6 and 5.3eV bulk WF, respectively). Reduction of the dielectric is observed by X-ray photoemission spectroscopy where the formation of a Hf sub-oxide peak is observed after annealing a fully oxidized HfO_2/Re or Pt stack [10]. Although this reaction is thermal dynamically unfavorable, but a catalytic decomposition of HfO_2 due to hydroxyls (OH impurities) will enhance the decomposition of HfO_2 by stabilizing the formation of charged O vacancies.

$$HfO_2H_{2x} + Me \rightarrow HfO_{2-x} + Me + xH_2O \uparrow$$

This reaction is also coupled with a electrostatic shift in the Hf 4*f* and O 1*s* core level bonds due to the charged defects formed, and has been suggested to induce E_f-pinning with these states (O vacancies), driving the E_f toward the conduction band and reduce the EWF observed by C-V measurements.

3.3.2 Extrinsic defect states: Oxygen vacancy model and interface dipole formation

High WF electrodes such as Pt and Re are reported to exhibit much lower EWF on high-k due to formation of a interface dipole at the metal/high-k interface. Due to the higher electronegativity of these metals (Pt: 2.28) versus Hf (1.3), a interface bonding configuration of Pt-Hf or Pt-V_o(oxygen vacancy)-Hf could result in electron transfer to Pt

side and thus form a dipole, and reduce the EWF (Figure 3.4(a)). Through process condition controls, passivation of this interface with more electronegative O atoms through O_2 annealing has shown to increase the EWF after reducing the concentration of such defects (Figure 3.4(b)). These learning also supports that connection with oxygen vacancies in the dielectric is the source of the interface charge exchange [7-9].

3.4 COMBINATION OF CHARGE NEUTRALITY MODEL AND OXYGEN VACANCY MODEL

An "general theory" of metal EWF based on a combination of the MIGS Φ_{CNL} concept (intrinsic) as well as the O vacancy contributions (extrinsic) is proposed to apply for all electrodes [13]. It suggest a new Φ_{CNL} which is the energy level where interfacial electron transfer is cancelled with interfacial hybridization, and thus depends on the amount of metal (M)-Hf versus metal-O interactions. As described in Figure 3.5, n-type metals with high O reactivity, mainly consist of M-O-Hf bonds; while in p-type metals M-Hf bonds dominate. The Φ_{CNL} thus follows the below relationship and will depend on the electrode interfacial bond number (number of metal-Hf bonds $|t_{M\text{-}Hf}|$ versus metal-O-Hf bonds $|t_{M\text{-}O}|$, and the density of occupied and unoccupied states in the metal (D_{occ}, D_{unocc}):

$$\phi^{G}_{CNL}=E_{VB}+E_{g}D_{unocc}N_{O}|t_{M\text{-}O}|^{2}/(D_{unocc}N_{O}|t_{M\text{-}O}|^{2}+D_{occ}N_{Hf}|t_{M\text{-}Hf}|^{2})$$

Therefore using the MIGS model to predict the EWF on high-k, results will be dependent on the electrode material, and the EWF vs bulk WF plot should not follow the traditional linear relationship (Section 3.2.1) due to the varied Φ_{CNL}.

3.5 ADDRESSING INTRINSIC FACTORS OF FERMI-LEVEL PINNING: COMPARISON OF TERRACED OXIDE EWF RESULTS WITH MIGS MODEL

3.5.1 Approach for study and experimental details

An accurate and systematic study of the EWF is required to identify the existence of an intrinsic contribution on EWF. Therefore, the terraced oxide method is used to eliminate ambiguities in EWF extraction on all samples studied. To separate out extrinsic contributions such as interfacial instability/reaction with the dielectrics, the study is focused on electrodes with high thermal stability with the high-k dielectric, such as metal-nitrides [16]. All samples have gone through a thermal budget to guarantee interfacial chemical bonding (the M-Hf or M-O-Hf bond formation) between the metal/high-k for the aforementioned extrinsic charge states to apply, and prevent the formation of a physically-absorbed (physi-sorbed) interface.

3.5.2 Comparison of EWF with MIGS model

Using the assumption that the metal EWF on SiO_2 equals, or has a 1:1 correlation with the vacuum WF [4], we plot in Figure 3.6 the extracted EWF of a series of electrodes on HfO_2 and $HfSiO_x$ (20% SiO_2) versus the EWF on SiO_2. Also with comparison with the MIGS trend line of S=0.53, and the 1:1 ideal correlation of S=1. The EWF results for HfO_2 and $HfSiO_x$ both show a near parallel relationship to the 1:1 ideal slope, with a ~100meV shift increase, possibly due to the stack charges described in Chapter 2.3.1. This parallel relationship suggests for thermally stable electrodes, **intrinsic** E_f-pinning is **not** the dominant factor controlling EWF, and EWF is not limited by the MIGS trend line. Interestingly, the near linear extraction of EWF results (EWF results for metals fall on same trend line, and not impacted by varied Φ_{CNL}) may also suggest the

varied Φ_{CNL} model described in Section 3.4 does not apply for these thermally stable electrodes.

3.6 REVISION OF MIGS THEORY

Due to discrepancy in experimental results in literature, Robertson et al. [17] reported ideal modeling of the metal/high-k barrier height to estimate the EWF. They propose the metal/high-k barrier height should be highly dependent on the metal/high-k interface configurations. The HfO_2 surface could be terminated with the polar-O (100) interface and has only M-O bonds, or exhibit a non-polar (110) interface with both M-O and M-M' bonds. It is believed that the most stable interface is metal system dependent [13], but in all will depend on the O chemical potential. Barrier height calculations can be modeled through CASTEP pseudo-potential total energy calculations, where the valance band offset (VBO) between is obtained from modeling of the valance band density of states. VBO is found to be larger for (110) than (100) due to interface dipole (Figure 3.7). Also, for given interface, slope S~1. Hence metal's EWF in principle should span Si gap. However, if a preferred orientation exists for a certain metal electrode to achieve stability ((100) for n-metals, (110) for p-metals), the VBO trend may follow the dashed line in Figure 3.7, and appear to reduce the slope to S~0.5. This could be consistent with the experimental EWF observations, and give the impression of an shallow slope. However, this suggests the MIGS model should not be universal, and cannot be applied to explain all metal EWF simply from intrinsic high-k interface states. Experimentally, the high-k after high thermal budgets are normally monoclinic with a preferred phase of (111) [18], and more modelling work needs to be performed to accurately predict the VBO for series of metal gate electrodes.

3.7 CONCLUSIONS

Through systematic discussion of literature reported models, and avoiding the pitfalls in the analysis. Our observations suggests after separating extrinsic factors, an intrinsic E_f-pinning should not limit EWF tuning on high-k. Figure 3.8 shows the EWF for vast material systems investigated with the terraced oxide method, and a similar range in EWF change on high-k and SiO_2 is consistently observed. Revision of the MIGS theory by Robertson et al. also agrees that the metal WF should in theory span the total Si band gap.

3.8 FIGURES

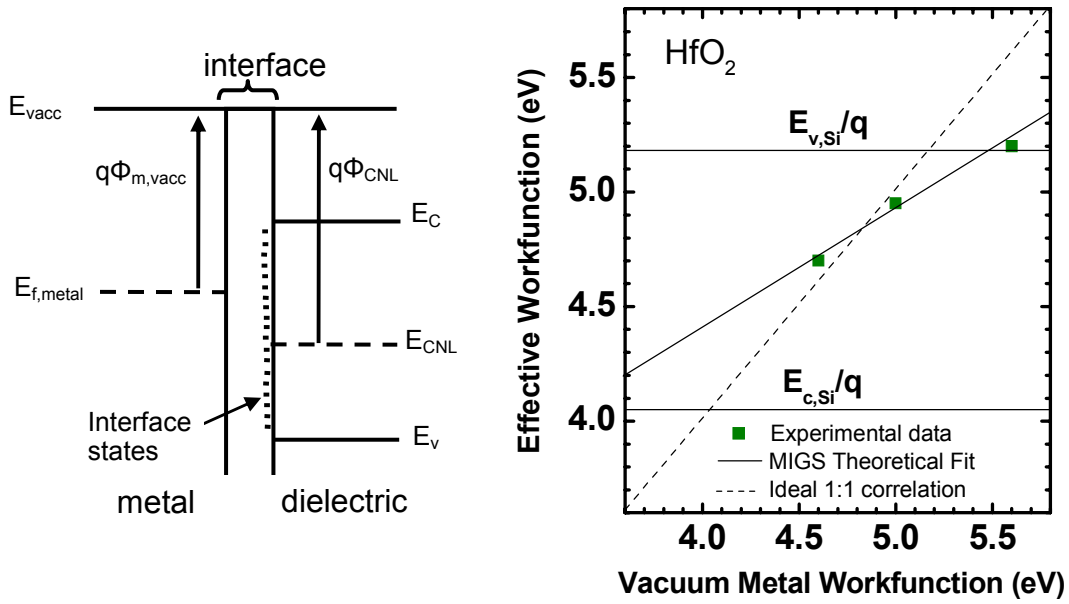


Figure 3.1 MIGS model predicted EWF on HfO_2 .[4]

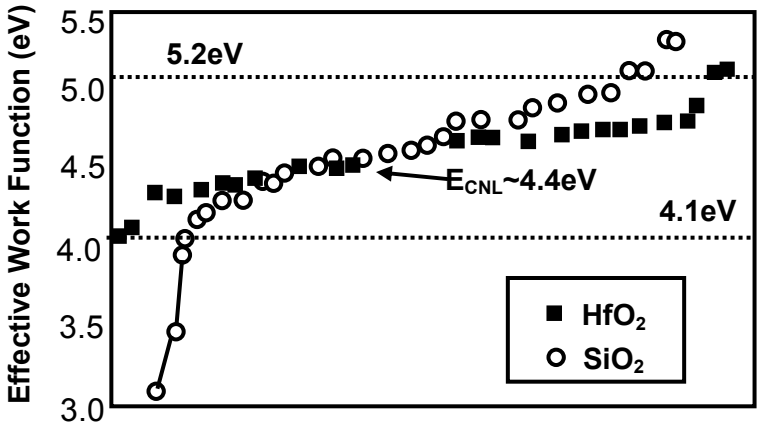


Figure 3.2 Plot of EWF for various metals on HfO_2 and on SiO_2 showing EWF shift toward the empirically calculated Φ_{CNL} of HfO_2 ~4.4eV. [3]

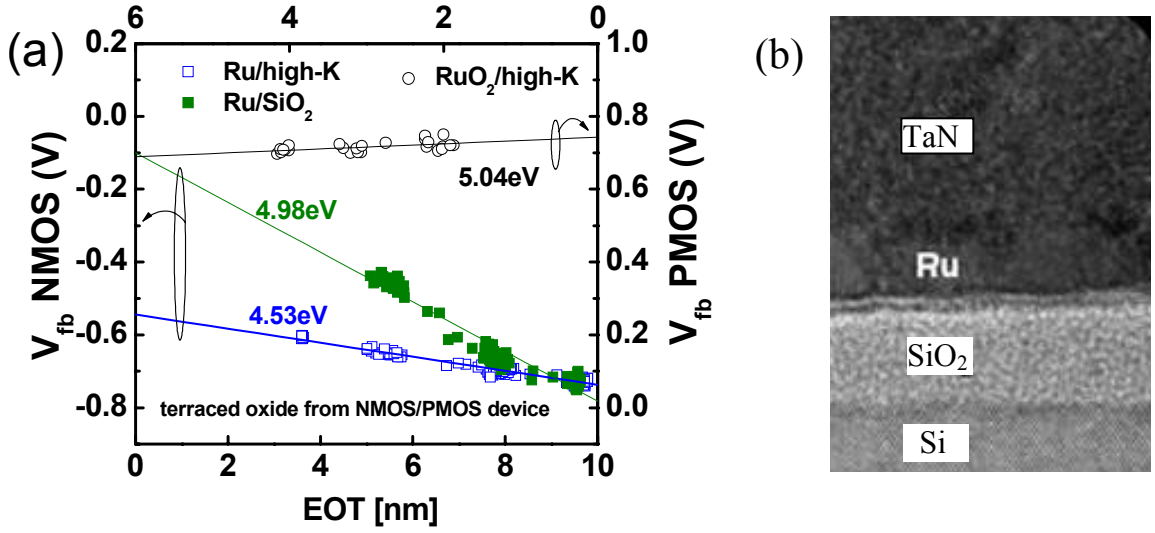


Figure 3.3 **(a) Vfb-EOT plot for EWF of Ru on SiO_2 compared with high-k dielectrics, and RuO_2 on high-k dielectrics (b) High resolution TEM image showing interaction between Ru and SiO_2 dielectric at elevated temperatures [12].**

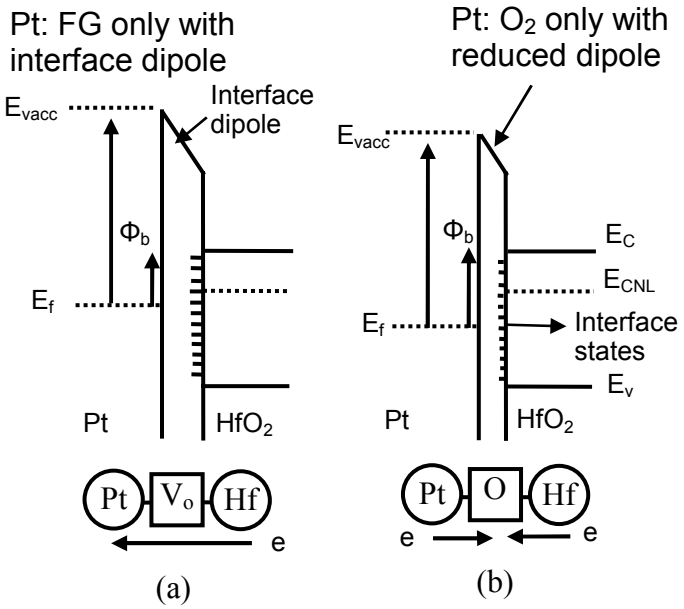
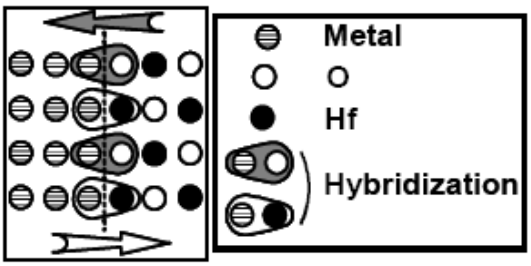


Figure 3.4 **(a) Schematic of the interface dipole formation for forming gas (FG) only and (b)after O_2 anneal conditions [8]**



(a)

mainly M-O-Hf bonds	Si, Al, Ti, Zr,Ta TaN TaC
Both M-Hf and M-O-Hf bonds	Au, Ni, Pt, Re Ag, W, Ru

(b)

Figure 3.5 **Schematic illustrating (a) Atomistic illustration of balanced situation of interface dipoles induced by interface metal-O and metal-Hf hybridization at the energy of Φ_{CNL}. (b) Preferred interface bonding for various metals. [13] (K. Shiraishi, et al., IEDM 2005, © 2005 IEEE)**

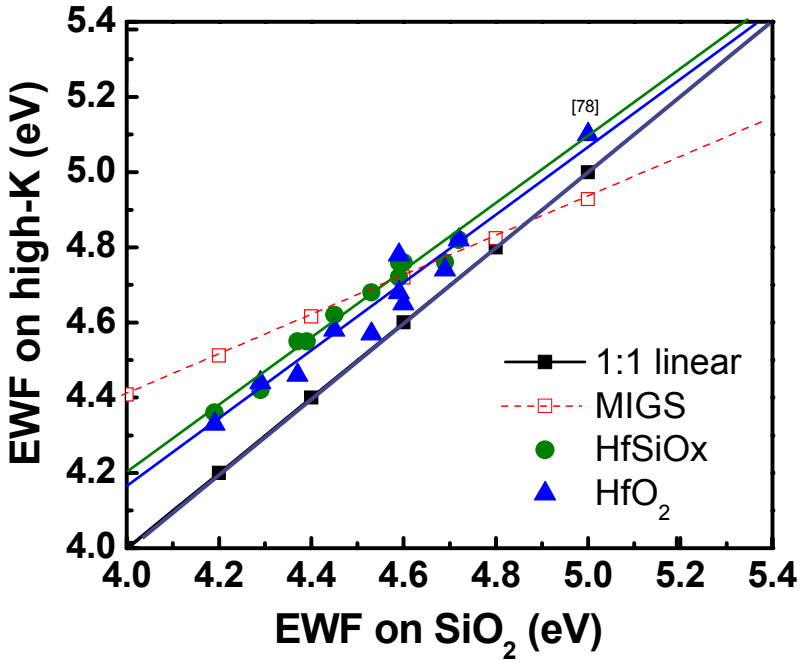


Figure 3.6 **The extracted EWF of a series of electrodes on HfO_2 and $HfSiO_x$ (20% SiO_2) versus the EWF on SiO_2, for comparison with the MIGS trend line with S=0.53, and the 1:1 ideal correlation with S=1.**

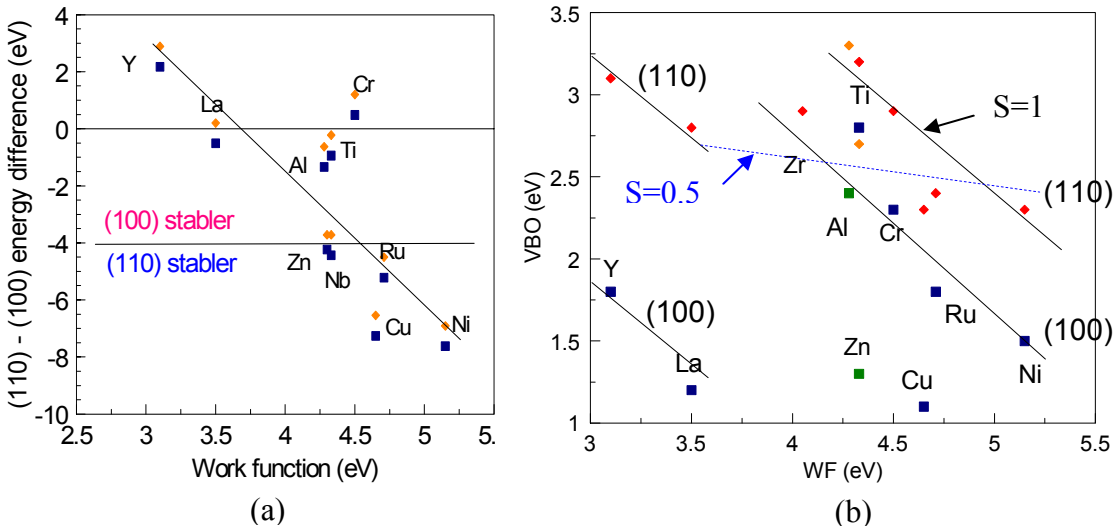


Figure 3.7 **Model results showing (a) energy difference between (110) and (100) interface of HfO_2 in contact with various metals, showing a preferred stability phase. (b) Valance band offset modeling for barrier height calculations of various metals on HfO_2 (110) and (100) interfaces. Most metals fall on solid trend line with S=1. Dashed line would be the trend considering the stable interface (S=0.5) [17]**

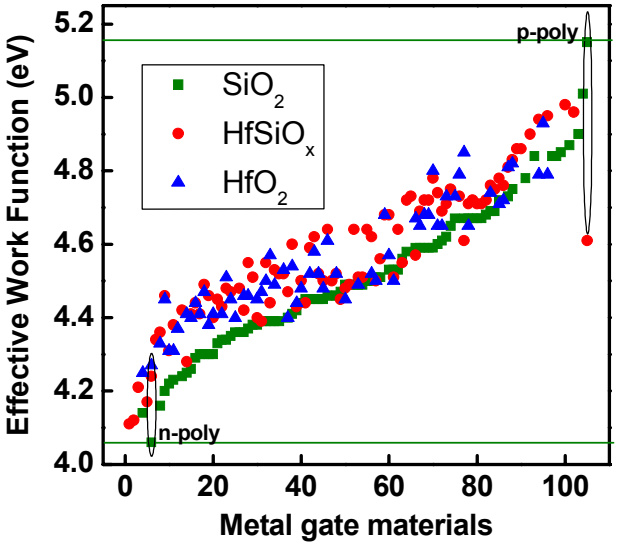


Figure 3.8 **EWF of various metal electrode materials investigated with the terraced oxide method.**

3.9 REFERENCES

[1] S. B. Samavedam, L. B. La, P. J. Tobin, B. White, C. Hobbs, L. R. C. Fonseca, A. A. Demkov, J. Schaeffer, E. Luckowski, A. Martinez, M. Raymond, D. Triyoso, D. Roan, V. Dhandapani, R. Garcia, S. G. H. Anderson, K. Moore, H. H. Tseng, C. Capasso, O. Adetutu, D. C. Gilmer, W. J. Taylor, R. Hegde, and J. Grant, "Fermi level pinning with sub-monolayer MeOx and metal gates [MOSFETs]," *Electron Devices Meeting, 2003. IEDM '03 Technical Digest. IEEE International*, pp. 13.1.1-13.1.4, 2003.

[2] C. Ren, H. Y. Yu, J. F. Kang, Y. T. Hou, M. E. Li, W. D. Wang, D. S. H. Chan, and D. L. Kwong, "Fermi-level pinning induced thermal instability in the effective work function of TaN in TaN/SiO2 gate stack," *Ieee Electron Device Letters*, vol. 25, pp. 123-125, 2004.

[3] J. Schaeffer, C. Capasso, L. R. C. Fonseca, S. Samavedam, L. B. La, J. Smith, S. Dakshina-Murthy, D. C. Gilmer, Luckowski, Y. Liang, S. Kalpat, B. Adetutu, H. H. Tseng, Y. Shiho, A. Demkov, R. Hegde, W. J. Taylor, R. Gregory, J. Jiang, E. Luckowski, M. Raymond, K. Moore, D. Triyoso, D. Roan, B. White, and P. J. Tobin, "Challenges for the integration of metal gate electrodes," *IEEE Electron Device Meeting*, 2004.

[4] Y. C. Yeo, T. J. King, and C. M. Hu, "Metal-dielectric band alignment and its implications for metal gate complementary metal-oxide-semiconductor technology," *Journal of Applied Physics*, vol. 92, pp. 7266-7271, 2002.

[5] Y. C. Yeo, P. Ranade, T. J. King, and C. M. Hu, "Effects of high-kappa gate dielectric materials on metal and silicon gate work functions," *Ieee Electron Device Letters*, vol. 23, pp. 342-344, 2002.

[6] H. Y. Yu, C. Ren, Y. C. Yeo, J. F. Kang, X. P. Wang, H. H. H. Ma, M. F. Li, D. S. H. Chan, and A. L. Kwong, "Fermi pinning-induced thermal instability of metal-gate work functions," *Ieee Electron Device Letters*, vol. 25, pp. 337-339, 2004.

[7] E. Cartier, F. R. McFeely, V. Narayanan, P. Jamison, B. P. Linder, M. Copel, V. K. Paruchuri, V. S. Basker, R. Haight, D. Lim, R. Carruthers, T. Shaw, M. Steen, J. Sleight, J. Rubino, H. Deligianni, S. Guha, R. Jammy, and G. Shahidi, "Role of oxygen vacancies in V/sub FB//V/sub t/ stability of pFET metals on HfO/sub 2/," *VLSI Technology, 2005. Digest of Technical Papers. 2005 Symposium on*, pp. 230-231, 2005.

[8] J. K. Schaeffer, L. R. C. Fonseca, S. B. Samavedam, Y. Liang, P. J. Tobin, and B. E. White, "Contributions to the effective work function of platinum on hafnium dioxide," *Applied Physics Letters*, vol. 85, pp. 1826-1828, 2004.

[9] Y. Liang, J. Curless, C. J. Tracy, D. C. Gilmer, J. K. Schaeffer, D. H. Triyoso, and P. J. Tobin, "Interface dipole and effective work function of Re in Re/HfO[sub 2]/SiO[sub x]/n-Si gate stack," *Applied Physics Letters*, vol. 88, pp. 072907, 2006.

[10] M. Copel, R. P. Pezzi, D. Neumayer, and P. Jamison, "Reduction of hafnium oxide and hafnium silicate by rhenium and platinum," *Applied Physics Letters*, vol. 88, pp. 072914, 2006.

[11] L. Pantisano, T. Schram, Z. Li, J. G. Lisoni, G. Pourtois, S. D. Gendt, D. P. Brunco, A. Akheyar, V. V. Afanas'ev, S. Shamuilia, and A. Stesmans, "Ruthenium gate electrodes on SiO[sub 2] and HfO[sub 2]: Sensitivity to hydrogen and oxygen ambients," *Applied Physics Letters*, vol. 88, pp. 243514, 2006.

[12] H. N. Alshareef, H. C. Wen, H. Luan, K. Choi, H. R. Harris, Y. Senzaki, P. Majhi, B. H. Lee, B. Foran, and G. Lian, "Temperature dependence of the work function of ruthenium-based gate electrodes," *Thin Solid Films*, vol. article in press Temperature dependence of the work function of ruthenium-based gate electrodes, 2006.

[13] K. Shiraishi, Y. Akasaka, S. Miyazaki, T. Nakayama, T. Nakaoka, G. Nakamura, K. Torii, H. Furutou, A. Ohta, P. Ahmet, K. Ohmori, H. Watanabe, T. Chikyo, M. L. Green, Y. Nara, and K. Yamada, "Universal theory of workfunctions at metal/Hf-based high-k dielectrics interfaces - guiding principles for gate metal selection," *Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International*, pp. 39-42, 2005.

[14] H. Yang, Y. Son, S. Baek, H. Hwang, H. Lim, and H.-S. Jung, "Ti gate compatible with atomic-layer-deposited HfO[sub 2] for n-type metal-oxide-semiconductor devices," *Applied Physics Letters*, vol. 86, pp. 092107, 2005.

[15] H. C. Wen, P. Lysaght, H. N. Alshareef, C. Huffman, H. R. Harris, K. Choi, Y. Senzaki, H. Luan, P. Majhi, B. H. Lee, M. J. Campin, B. Foran, G. D. Lian, and D. L. Kwong, "Thermal response of Ru electrodes in contact with SiO2 and Hf-based high-k gate dielectrics," *Journal of Applied Physics*, vol. 98, 2005.

[16] H.-C. Wen, K. Choi, P. Majhi, H. Alshareef, C. Huffman, and B. H. Lee, "A systematic study of the influence of nitrogen in tuning the effective work function of nitrided metal gates," presented at VLSI Technology, 2005. (VLSI-TSA-Tech). 2005 IEEE VLSI-TSA International Symposium on, 2005.

[17] J. Robertson, "Invited talk at EMRS 2006," 2006.

[18] G. Pant, A. Gnade, M. J. Kim, R. M. Wallace, B. E. Gnade, M. A. Quevedo-Lopez, and P. D. Kirsch, "Effect of thickness on the crystallization of ultrathin HfSiON gate dielectrics," *Applied Physics Letters*, vol. 88, pp. 032901, 2006.

CHAPTER 4

UNDERSTANDING FACTORS CONTRIBUTING TO THE EWF OF METAL ELECTRODES

4.1 INTRODUCTION

The EWF of metal gate electrodes ideally should only be dependent on bulk/vacuum work function of the materials. However, we've observed the relationship is not so ideal in a MOS structure. The concern of WF deviation due to inaccurate EWF extraction had been addressed in Chapter 2, where the terraced oxide method is proposed for EWF extraction on high-k. In Chapter 3, an intrinsic E_f-pinning effect is found not to limit EWF tunability on high-k, and any E_f-pinning effects has been clarified to be mainly extrinsic. Extrinsic contributions from the overall gatestack have been found to impact the overall measured EWF due to interdiffusion/reaction between layers, processing conditions in the fabrication of the devices, or induce stack charges. Such complexity has obstructed the identification of band-edge metal electrode systems, and the understanding of EWF control on high-k dielectrics. From an engineering perspective, it is critical to perform a systematic study of key factors effective in EWF tuning, in effort to identify material systems and integration pathways that hold promise in engineering metal-high-k stacks using the conventional gate first process.

Breakdown of the V_{fb} equation below has separated contributions to V_{fb} (and the extracted EWF) into the following factors:

$$V_{fb} = (\underline{\underline{\Phi'_{ms}}} - \frac{Q_i * EOTh}{\varepsilon_{ox}} - \frac{\rho_b * (\varepsilon_h / \varepsilon_{ox}) * EOTh^2}{2 * \varepsilon_{ox}} + \underline{\underline{\Delta D + \Delta Q}}) - \frac{Q_f * EOT}{\varepsilon_{ox}}$$

The metal material properties effecting the bulk work function contributes to the Φ_{ms} term. Intrinsic dielectric stack charges at the high-k/SiO_2 and bulk of the high-k effects influence the Q_i, Q_f, and ρ_b term. Compared to the ideal V_{fb} equation, additional factors are considered, ΔD is the dipole term formed possibly between the metal/high-k dielectric or within the dielectric interfaces, ΔQ are the additional charges induced in the dielectric/stack due to extrinsic sources. Any changes in these terms will result in variation in the extracted EWF. In this chapter, a more systematic investigation of the factors contributing to the measured EWF is performed.

4.2 CONTROLLING METAL BULK WORK FUNCTION COMPONENT

4.2.1 Pure metal and metal alloys

The bulk (vacuum) work function for materials should ideally control the EWF for pure metals and alloy systems. Two examples of such systems are given below to show the impact of bulk work function, and its controllability on the EWF.

4.2.1.1 Complete solid solution

NMOS capacitors with the terraced oxide structures were processed, and topped with a 3nm HfO_2 high-k dielectric for EWF evaluation on SiO_2 and high-k. Ta-W alloys of various compositions were deposited by a low damage physical vapor deposition (PVD) process, and capped by TaN and poly-Si followed by rapid thermal annealing up to 1000^oC to simulate the gate first transistor process.

The binary phase diagram for Ta-W alloys shown in Figure 4.1(a) [1], suggests that thermal dynamically the Ta-W alloy system forms a complete solid solution, and thus all material properties should follow Vegard's Law and exhibit a linear relationship with %

composition of Ta to W. Eliminating phase formation, or phase separation, enables a better evaluation of the EWF of a material system. To investigate whether the EWF of Ta-W alloys exhibits the same linear relationship, the EWF was extracted from terraced oxide wafers on both SiO_2 and high-k (Figure 4.2(b)). In the case of the SiO_2 gate dielectric, EWF of the pure Ta and W electrodes exhibit excellent agreement with their expected bulk work function values (4.3eV for Ta, and 4.5 for W) [2]. However, EWF of the pure Ta electrode in the high-k stack is increased to 4.48eV, exactly as could be expected if Fermi-level pinning effect is occurring. Further observation of the Ta-W alloy electrodes, however, shows a near linear relationship of the EWF with %Ta composition, and a similar degree of the EWF change is observed in the stacks with both SiO_2 and high-k dielectrics. The Ta-W EWF on high-K is not impacted by the Fermi-level pinning phenomena or otherwise will be constant ~4.5 independent of the composition changes.

A careful look at the flatband voltage (V_{fb})-effective oxide thickness (EOT) plot for terraced oxide EWF extraction on SiO_2 and high-k in Figure 4.2 (a) and (b), respectively, enables more understanding of the physics. A linear fit of the V_{fb}-EOT plots, which exhibit near parallel shifts for different alloy compositions, as well as small slopes of the V_{fb}-EOT dependencies (low fixed interface charges (Q_f)), suggest accurate EWF extraction, good sensitivity of the EWF to % composition change, and minimum impact of the SiO_2/Si quality. First, since the starting terraced oxide thicknesses are the same, similar EOTs are expected in stacks with different Ta-W compositions. However, the W gated electrode exhibits higher EOTs, and an addition of Ta reduces the maximum EOT (focus on max EOT regime). The pure Ta film shows an EOT reduction of nearly 2nm. This reduction of EOT suggests interfacial reaction between the Ta containing electrode

and SiO_2, where a high energy of oxide formation for Ta limits the thermal stability of Ta on SiO_2 dielectrics. Reduction of the SiO_2 to form a TaOx-like interface, which has a higher k value, could result in the EOT decrease. In this case, the EWF value of the pure Ta electrode in the SiO_2 dielectric stack is controlled by the interfacial reaction. Physical observation of the interfacial reaction is shown in Figure 4.3(a), where an interface is observed between the Ta and SiO_2 region. W electrodes are known to be thermally stable with SiO_2 and do not exhibit the interfacial reaction. Based on the EOT results, doping/alloying of Ta with W is shown to significantly suppress this interaction. Interestingly, regardless of interfacial reaction, the EWF extracted is still consistent with that expected from its bulk value, suggesting minimum impact of TaO_x charges on V_{fb}.

Reduced EOT and interfacial interaction are not observed on the high-k dielectrics (Figure 4.3(b)), suggesting better stability of the Ta to the high-k interface. The Ta-W alloy regime also still exhibit the same degree of tunability as the SiO_2 results. However, degradation of the high-k due to Ta diffusion is shown in Figure 4.4, where the leakage current densities of the Ta, Ta-W alloy, and W metal gate/high-k stacks are compared in the thin EOT regime. The Ta gated stack has significantly higher leakage than the W or Ta-W samples. No leakage degradation is observed for the alloys suggest the thermal stability of a reactive electrode can be improved by alloying with more stable materials, and may limit Ta diffusion. Ta diffusion into the high-k matrix could impact the V_{fb} result by modulating the dielectric charge, and contribute to the ΔQ term in the V_{fb} equation. This may explain the increased EWF for pure Ta. More careful characterization of materials is needed to determine the interfacial reactions at the Ta-W alloy and high-k dielectrics to separate the contributions of the electrode, metal/high-k interface, and dielectric charge to the EWF.

The Ta-W alloy is an excellent system with which to demonstrate contributions to the measured EWF by the bulk WF, interface reaction, and dielectric (charge) modulation.

4.2.1.2 Inter-metallic compounds

The novel Ru-Hf alloy system, with the combination of high work function Ru (5.0eV) [3] and low work function Hf [2] is an example of materialistic phase control of the EWF. The use of Hf based electrodes in conjunction with Hf based dielectrics is of high interest from a material compatibility standpoint.

A fixed 40Å HfO_x was deposited on varying thickness of SiO_2 terraced oxide wafer. The Ru-Hf metal electrodes were co-sputtered on these dielectric stacks, and TiN/W was used as metal capping layers to form MOS capacitors. Ru-Hf alloys with varying composition were processed by co-sputtering Ru and Hf. Figure 4.5 shows the composition of Ru:Hf from Rutherford Backscattering Spectrometry (RBS) measurements. The Ru:Hf ratio is shown to be dependent on the Ru:Hf power ratio, and Ru% composition is tuned between 80~35%. However, since the phase stability diagram does not show complete solid solubility (Figure 4.6) [1], X-ray diffraction was used to study the phases for the varying compositions. Figure 4.7 is the X-ray diffraction pattern for the RuHf (3:1), RuHf (1:1), and RuHf (1:3). The pattern for RuHf (3:1) indicates pure Ru(111) (2θ~40.7^o) peak overlapping a potential RuHf(110) (2θ~39.4^o) peak. The spectrum of the RuHf (1:1) clearly shows the formation of stoichiometric RuHf phase, while the RuHf (1:3) shows a mix of RuHf and possible pure Hf which was oxidized to form HfO_2 at (2θ~28^o). Additionally, the spectrum indicates that the lattice spacing of the RuHf is expanded, indicating the possibility of excess Hf inclusion in the RuHf phase. The possibility of Hf inclusion provides the ability for additional Hf incorporation, and thus more space for work function tunability via composition change. Figure 4.8(a) is the

V_{fb}-EOT plot for the various Ru-Hf alloy compositions. The extracted work function values vary from 4.35 to 4.78 eV as the Ru content increases from 35% to 100%. NMOS C-V curves for the different metal gates, clearly show that there is parallel shift in the C-V (towards "n" type with increasing Hf), which is due to the shift in the effective work function of the gate electrode. Figure 4.8(b) is the EWF summary versus various Ru composition. Unlike the Ta-W system, the relationship is not linear, and is dominated by the phase, thus separated into a Ru controlled, and RuHf alloy phase controlled regime, consistent with the XRD phases. The range of EWF tunability of 400meV in this system is highly attractive for dual WF metal electrodes [4]. However, due to thermal stability concerns with the Ru as well as Hf material systems (Chapter 3), we can predict further annealing will result in interface reactions and interface controlled EWF.

4.2.2 Metal nitrides and metal silicon nitrides

Although some as-deposited elemental metals do exhibit near band-edge work function values, their tendency to react with the dielectrics has been limiting the thermal stability of both n-type (ex. Ta) and p-type (ex. Ru, Pt) electrodes. Most of the low workfunction materials (bulk form) are inherently reactive and hence cannot be used in their pure forms. Addition of constituents stabilizes the material and provide improved thermal stability. Certain additives to the metal, in particular, nitrogen (metal nitrides) and/or Si (metal silicides, ternary metal-Si-N) have been evaluated, and metal nitrides or silicides have been proposed to be preferred over pure metals as dual metal electrode candidates [5-8]. Many groups studied a fixed composition of metal nitrides and reported near mid-gap values for the EWF, and has postulated addition of N or Si to shift the EWF toward mid-gap. However, a systematic study of the influence of these additions on the effective work function of the candidate materials is lacking.

A multi-target sputter tool was used to reactively deposit nitrides of Hf, Ti, and Ta. Also, ternary systems (HfSiN, TaSiN, MoSiN) were deposited by co-sputtering the metals (and Si) in reactive nitrogen plasma. The flow rate of nitrogen in the plasma was tuned to incorporate varying amounts of nitrogen in the metals. MOS capacitors with these metals on silicon-dioxide and hafnium based oxides were processed to characterize the device properties and extract the EWF of the metal nitrides. The MOS capacitors were subjected to high temperature anneal (1000 ^{o}C 5 sec) similar to the activation anneals in transistor fabrication.

Metal nitrides

T**aN**: Figure 4.9(a) and (b) are the RBS composition scans and sheet-resistance values for TaNx deposited with varying N_2 flow rate in the plasma. Figure 4.10(a)(b) are the V_{fb}-EOT plots for the different compositions on silicon oxide and hafnium dioxides. Note, there is clear indication of increasing WF with increasing nitrogen content. Pure Ta has a bulk WF of ~ 4.25 eV, but is very reactive as we learned in Section 4.2.1.1. Adding nitrogen reduces its reactivity but shifts its work function towards mid-gap values. Figure 4.11 shows the C-V curves for the TaN metals with varying nitrogen content. The lateral shift in the curves with minimal observable stretch-out suggest that the effective work function of the metal gates are indeed being tuned without severely affecting the gate dielectric underneath. From the above data, it is evident that one may fabricate Ta based nitride with sufficient nitrogen to make it less reactive and at the same time achieve effective work function values appropriate for nMOS electrode.

In general, the addition of nitrogen increases the EWF, for both n-type metals (Hf, Ti, Ta) with vacuum WF=3.9-4.33 as well as midgap metals (Mo, W) with WF=4.55~4.6

(Figure 4.12). Contrary to popular beliefs, the EWF is not merging toward midgap. This is believed to be related to the increased electronegativity (X_M) of the film. [9] The vacuum work function (Φ_{vac}) exhibits a reasonable agreement with electronegativity with the relationship below:

$$\Phi vac = 2.27 X_M + 0.34$$

Nitrogen has an electronegativity value of 3.04, which is higher than that of our elemental metals (Hf=1.3, Ti=1.54, Ta=1.5, Mo=2.16, W=2.36). This also suggests the effect on the EWF from addition of other elements in row 2 of the periodic table (B, C, N, O) should also depend on their relative X_M, which is 2.04, 2.55, 3.04, 3.44, respectively, and agrees with values reported in [10]. EWF tunability by nitrogen control is ~200meV.

Metal-silicon-nitride

Amorphous materials, owing to the absence of grains and good diffusion barrier properties, are preferred over crystalline systems, since they exhibit less dependence of the effective work function on device processing conditions. Ternary films of the generic composition (early transition metal (TM))-Si-(nitrogen or oxygen) are likely to form amorphous or near-amorphous structures [11, 12]. Materials highlighted in Figure 4.13indicate compositions, which may form these near-amorphous systems due to self-limited grain growth mechanisms.

TiSiN, MoSiN and TaSiN ternary phase diagrams are shown in Figure 4.14. The tie line connecting 2 compounds in the binary systems (TM-N and Si-N) represent potential composition regimes wherein the ternary system may remain amorphous even after annealing due to limited nucleation and grain growth of the two immiscible phases [11]. From the XRD spectrums in Figure 4.15, reduction in the TM-N peaks after adding Si is observed for films after 1000^{o}C thermal treatment, which is consistent with

the formation of amorphous metal materials. No significant binary (crystalline) phase formation is detected for TaSiN, MoSiN, and TiSiN. The EWF of TaSiN extracted from terraced oxides is shown in Figure 4.16(a). The parallel V_{fb} vs. EOT trends for different %Si in the film clearly demonstrate the sensitivity of the work function extraction method to the film composition. Low fixed interface charge values (5E10~1E11/cm^2) are measured for both SiO_2 and $HfSiO_x$ gate dielectric films. EWF of TaSiN (Figure 4.16(b)) decreases with increasing atomic %Si. Based on this observation, a novel process was developed to deposit Ta-Si-N material with the EWF as low as 4.2eV even after the 1000^{o}C anneal, making it a suitable N-type metal candidate. Figure 4.18(a) shows the HRTEM images of TaSiN confirming its amorphous material structure. Decrease in the EWF values with increasing %Si was also observed in other ternary metal nitride systems such as PVD MoSiN and HfSiN. The EWF values decrease from 4.5eV (MoN) to 4.3eV (MoSiN) with increasing Si content (Figure 4.17(a)), and 4.5 (HfN) to 4.4 for HfSiN (Figure 4.17(b)). EELS scans across the gate stack did not indicate any diffusion of elements across the metal-dielectric interface for the TaSiN and HfSiN films. Hence, nitrogen induced fixed charges in the dielectric cannot be responsible for the reduction of the EWF value. A plausible explanation for the lower EWF values in these systems could be related to the Si-N like interface at the dielectric surface. Figure 4.18(b) shows the HRTEM of extremely Si rich versus a Ta rich TaSiN film. The extremely Si rich film exhibits some degree of phase separation after high thermal budgets. Figure 4.19 is the EWF for stacks with intentional deposition of various thickness PVD SiN on the terraced oxide prior to TaN electrode deposition. Reduction in the EWF ~200meV is observed consistent with that of Si rich TaSiN films.

Interestingly, CVD Ti-Si-N systems were evaluated also to study the effect of Si addition on EWF. The V_{fb}-EOT plots of CVD TiN and TiSiN are compared in (Figure

4.20). Here, an increase in the EWF of ~0.3 eV by incorporating Si has been observed for the TiSiN metals on both SiO_2 and $HfSiO_x$. The specific role of Si in altering the bonding structure of these ternary systems is not yet clear, but the role of the different reaction processes (CVD for TiSiN and PVD for MoSiN, TaSiN, HfSiN) may also be significant in determining the eventual nanostructure of the films. Out of many metal systems evaluated, amorphous TM-Si-N are identified and their EWF are reported in Figure 4.21. EWF of the amorphous metals with 1000^{o}C thermal budget can be tuned within a 600meV range (4.2~4.8eV) on both SiO_2 and high-k dielectrics. Other amorphous materials besides the TM-Si-N system are also of high interest for metal gate applications, and dual work function amorphous metal gates could be anticipated from proper engineering of amorphous metal materials.

4.3 IMPACT OF GATE STACK CHARGES ON EWF

Process induced charges is a critical term in impacting the extracted EWF. One typical source of process induced charges is from nitrogen during the high-k nitridation process. N has been reported to exhibit positive charge within the dielectric [13], and will lower the V_{fb}. An experiment is conducted using intentional plasma nitridation of the dielectric for N incorporation. Figure 4.22 shows the V_{fb}-EOT of a TaN/$HfSiO_x$/terraced oxide stack, where the dielectric is exposed to various plasma nitridation times. It is observed with longer nitridation, an lowering in the EWF is observed. Comparison of the V_{fb} shows a difference of ~0.2eV with 5s versus 60s nitridation. Utilizing the leakage current technique, we are able to extract the actual barrier height between TaN and $HfSiO_x$. Figure 4.23, shows the $\Delta\ln(J_g)/\Delta V_g$ relationship, where the peak voltage is the barrier height. Despite the differences in V_{fb} due to nitridation, no changes was observed

in the barrier height, suggesting the source of V_{fb} change is due to positive charges, possibly from the incorporated nitrogen.

Previous literature reports have shown implantation of N into Mo reduces the EWF from 5.0eV to 4.4eV, and proposed to be due to formation of Mo_2N at the dielectric interface [14]. However, the impact of N on the EWF, i.e. formation of metal nitrides, had been systematically here, and N is found to increase the bulk WF for various metal electrode systems, including Mo (section 4.2.2). Therefore, N incorporated from implantation may be distributed more in the dielectric, and positive charge formation in the dielectric could explain the EWF reduction toward n-type.

4.4 CONCLUSIONS

Systematic study has been performed to understand factors impacting the EWF. Bulk material composition tuning is effective, however, thermal stability concerns limit the use of bulk n/p-type band edge metals. Addition of N and/or Si is proven to improve the thermal stability, and is more favorable for bulk CMOS processing, however the degree of EWF span is limited to ~600meV. Some examples of extrinsic factors controlling EWF mentioned in Chapter 3 are discussed, and we find the metal/high-k interface is dominant in controlling the EWF. Therefore, application of interface engineering on high-k may be an attractive approach for EWF tuning toward the band-edge.

4.5 FIGURES

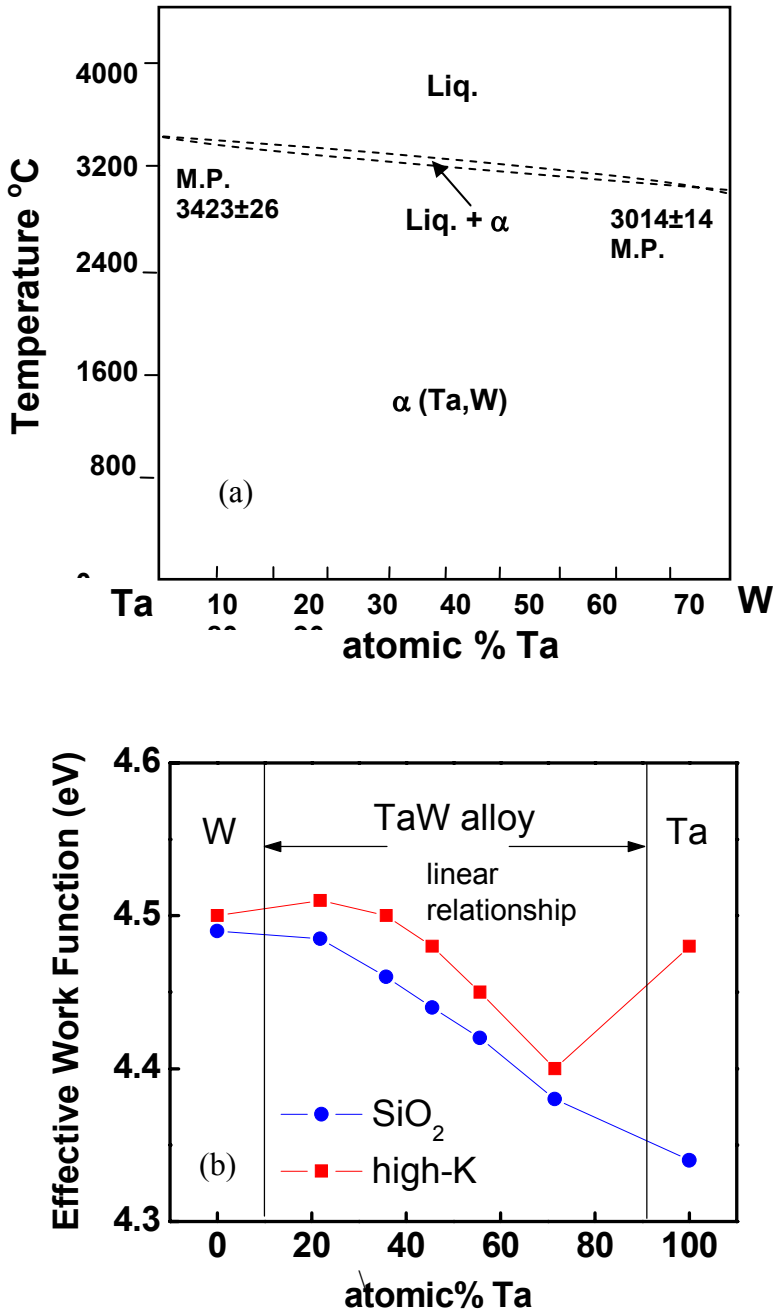
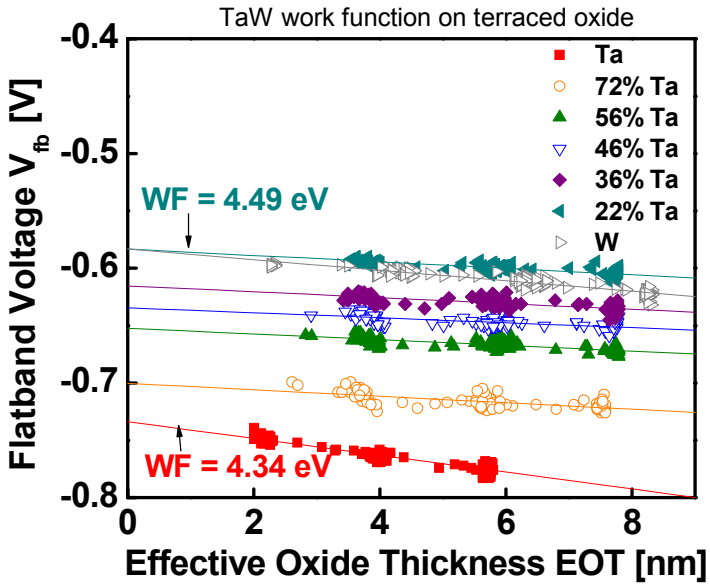
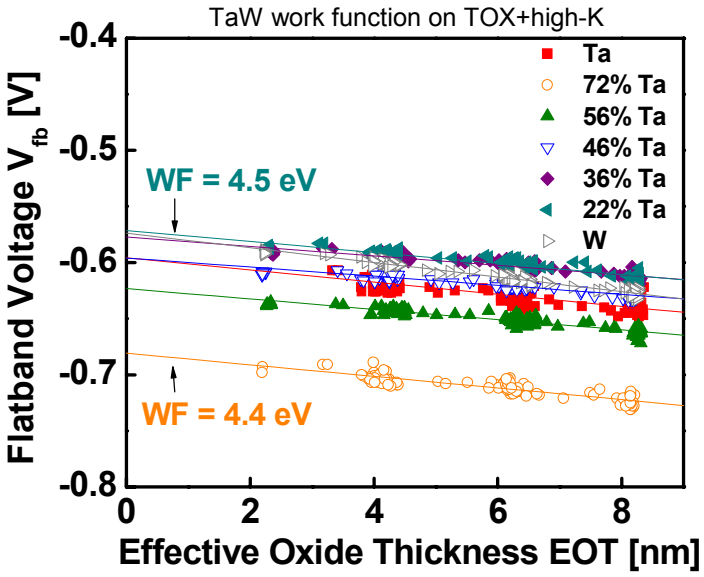


Figure 4.1 **(a) Phase diagram of the Ta-W binary alloy system based on reference [1]. A complete solid solution is observed. (b) The effective work function for Ta-W alloys on SiO_2 and high-k dielectrics as a function of varied atomic Ta%, showing linear relationship in the alloy region.**



(a)



(b)

Figure 4.2 The V_{fb} versus EOT relationship results used for effective work function extraction obtained on (a) terraced oxide and (b) terraced oxide + high-k stacks showing excellent linear extraction. Changes in EOT for the thickest EOT band within each wafer can be used to identify overall EOT changes.

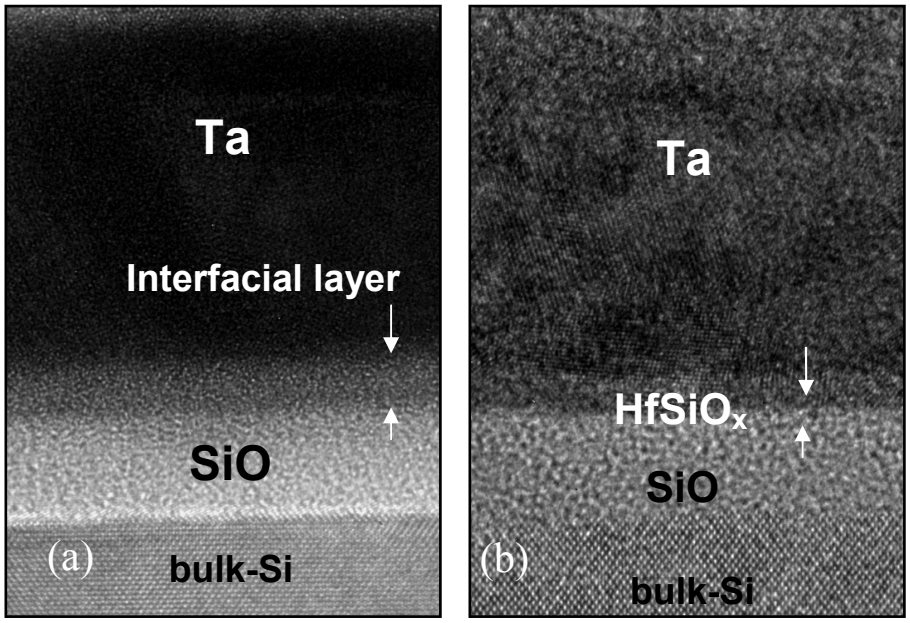


Figure 4.3 High resolution transmission electron microscopy (HRTEM) images of the (a) $Ta/SiO_2/Si$ and the (b) $Ta/HfSiOx/SiO_2/Si$ gate stack interfaces. Formation of an interface layer is observed between the Ta/SiO_2 interface.

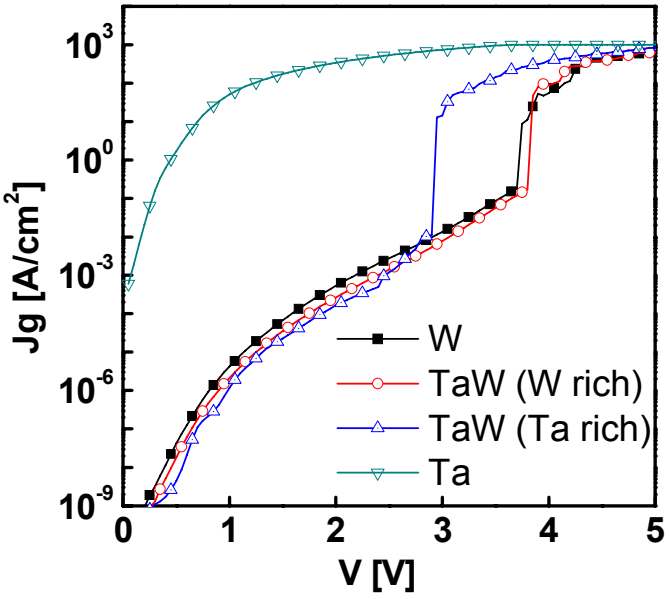


Figure 4.4 Leakage current density of W, Ta-W alloys and Ta metal electrodes on high-k. Higher leakage current is observed only with the Ta sample, suggesting degradation of the dielectric, while Ta-W alloys and pure W are similar.

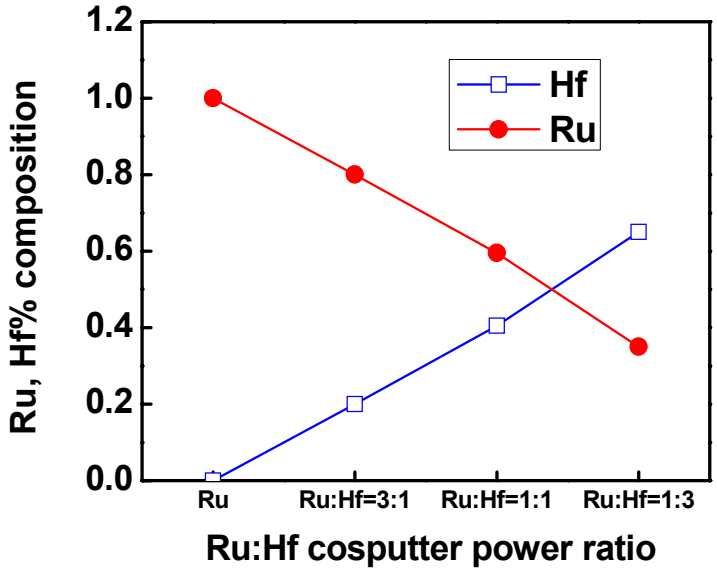


Figure 4.5 **RBS composition of RuHf alloy.**

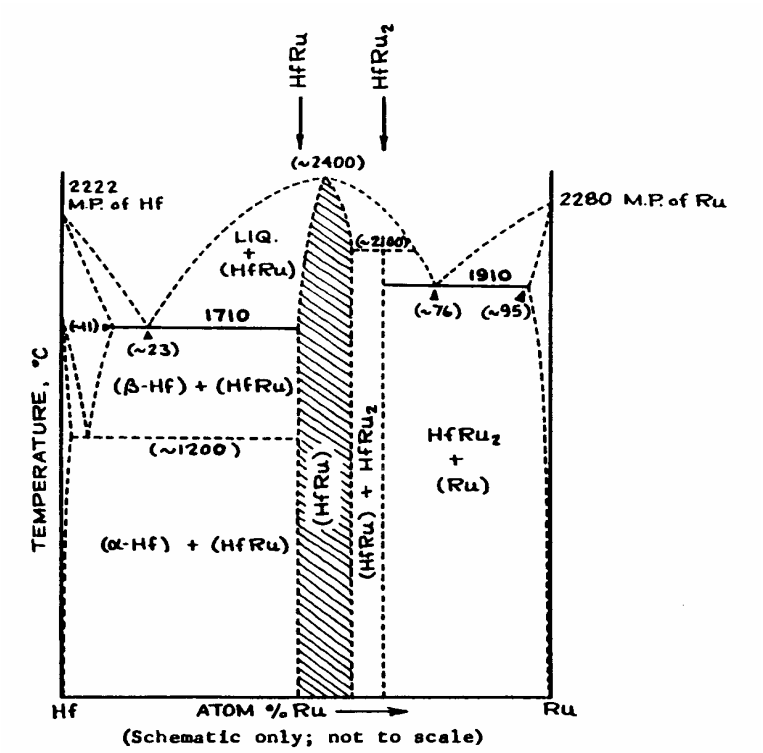
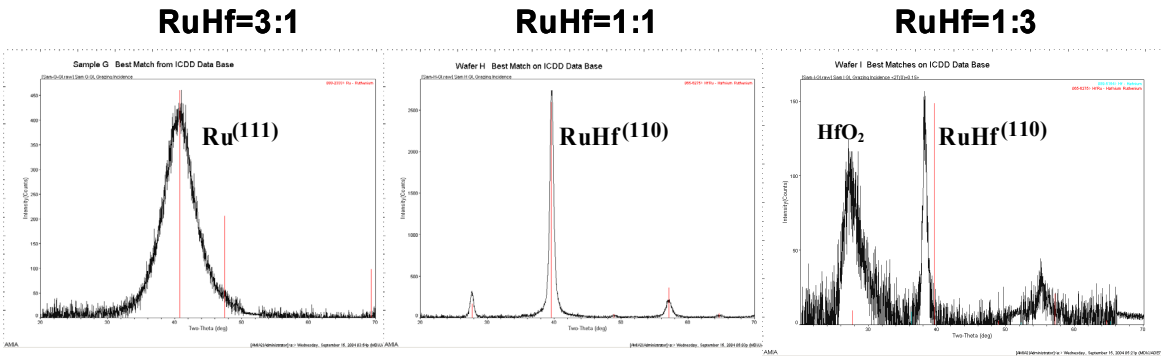


Figure 4.6 **Phase diagram of RuHf alloy system.[1]**



Ru- Ruthenium
Fm3m (Face Centered Cubic)

RuHf – Ruthenium Hafnium
Pm3m (Primitive Cubic)

appears to be Pm3m like RuHf, but with significant peak shifts (lattice spacing shifts)

Figure 4.7 XRD diffraction pattern for RuHf alloys of various composition

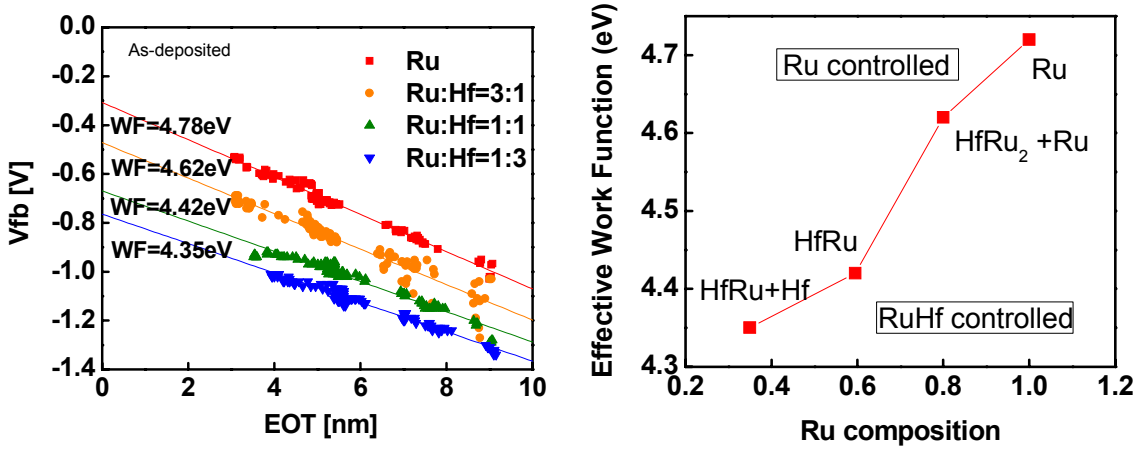


Figure 4.8 (a) V_{fb} vs. EOT plot for work function extraction of various Ru:Hf compositions as-deposited on terraced oxide + HfO_2. (b) EWF trend with varied Ru composition, trend with composition is not linear and dependent on dominant phase, is separated into Ru, and RuHf controlled regions.

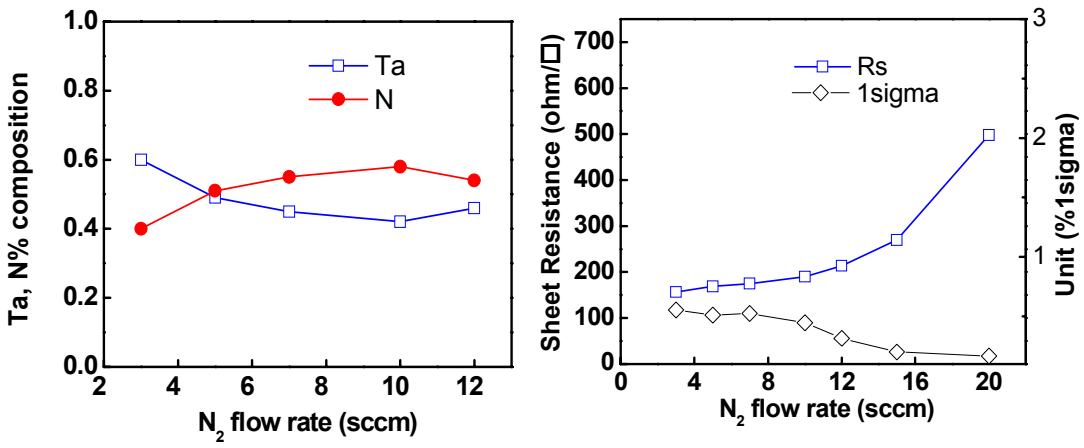


Figure 4.9 (a) RBS composition of Ta, N in TaN with varying N_2 flow rate. (b) Sheet resistance of TaN with varying N_2 flow rate.

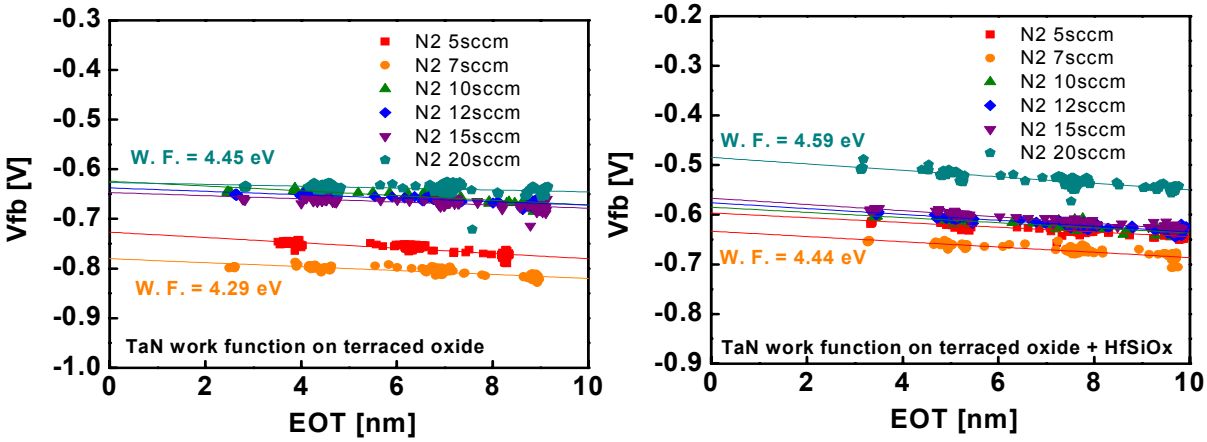


Figure 4.10 V_{fb} vs. EOT plot for work function extraction of TaN on (a) terraced oxide and (b) terraced oxide+ 30Å $HfSiO_x$.

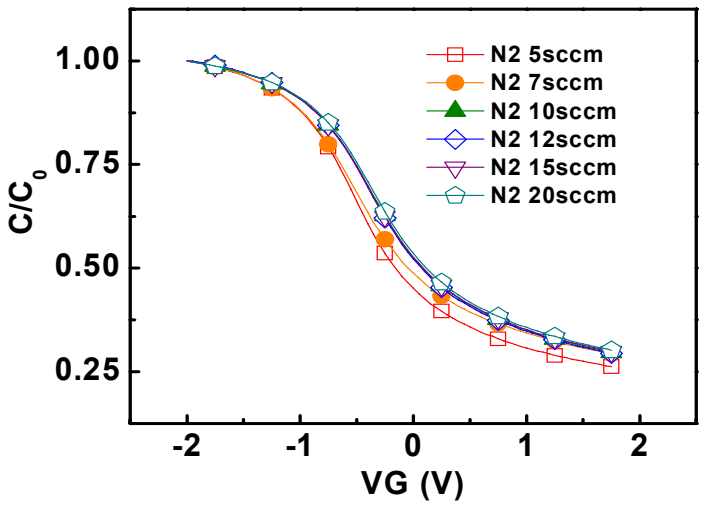


Figure 4.11 **Normalized C-V plot of TaN with varying N_2 flow rate on SiO_2.**

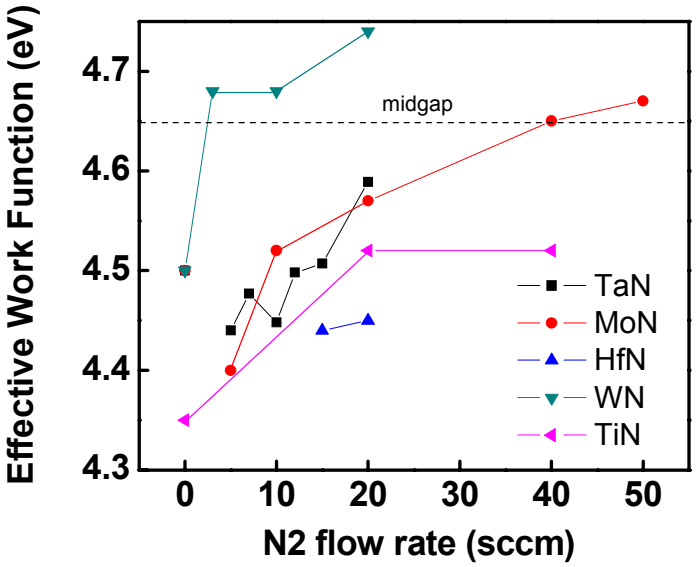


Figure 4.12 **Summary of EWF of metal nitride with varying nitrogen process flow rates.**

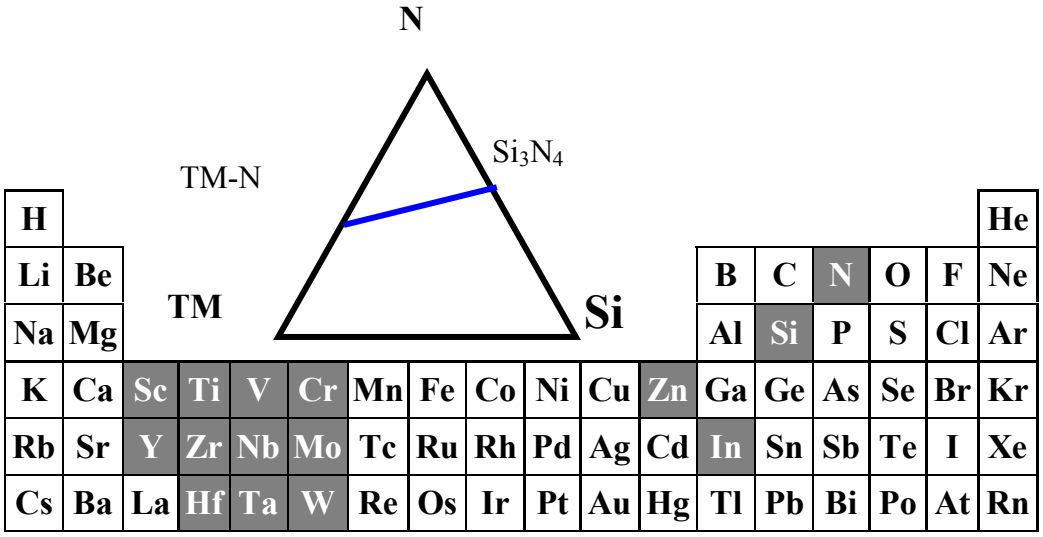


Figure 4.13 Ternary phase diagram of TM-Si-N systems. Periodic table of elements which form the quasi-binary TM-N, Si-N system [11].

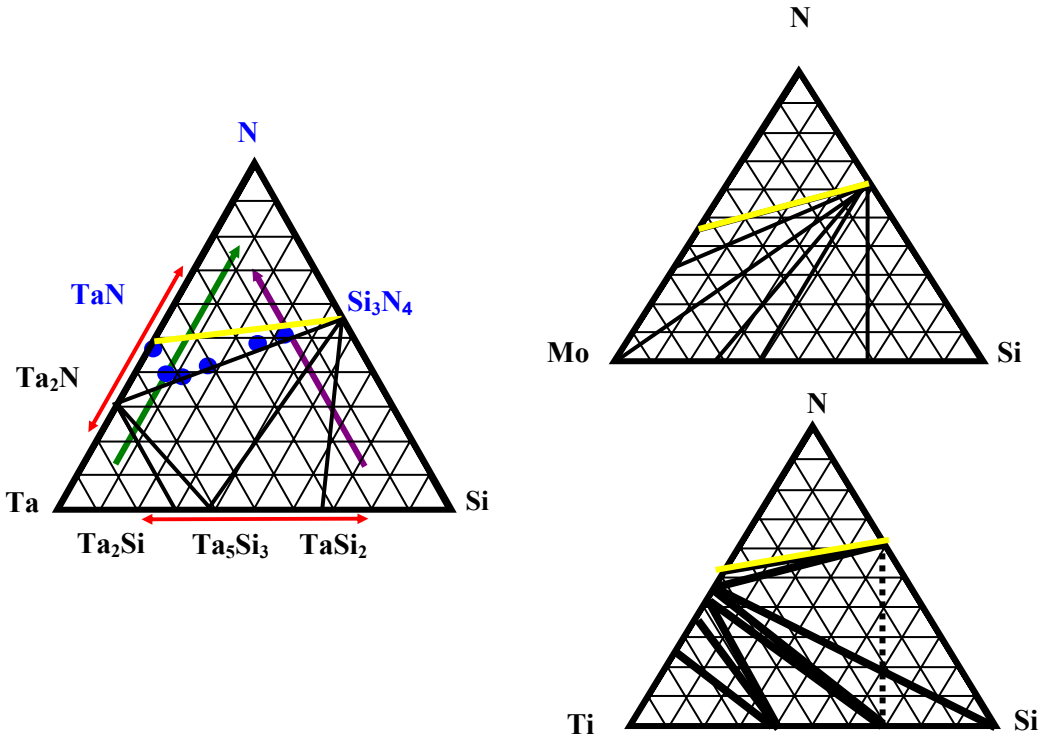


Figure 4.14 Ternary phase diagram for TiSiN, MoSiN and TaSiN and trend lines indicating regions evaluated.

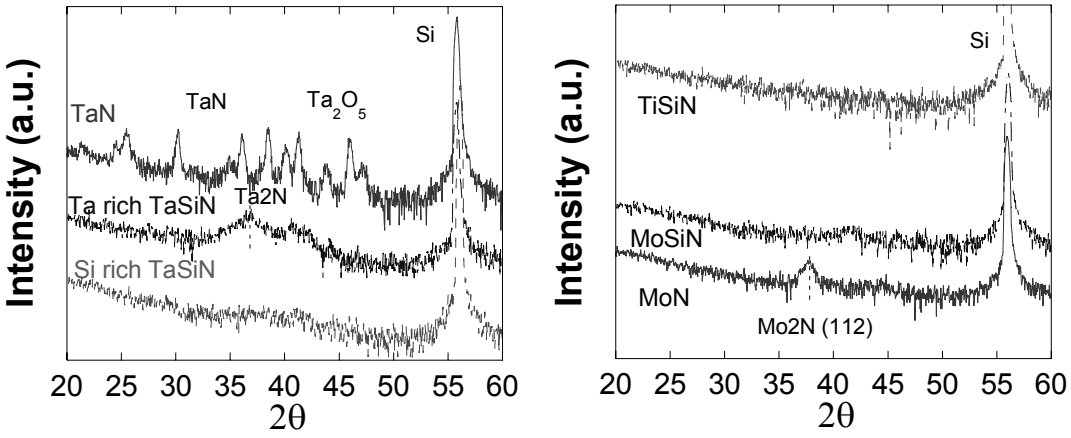


Figure 4.15 XRD spectrums for TM-Si-N films and their TM-N after a 1000°C thermal anneal.

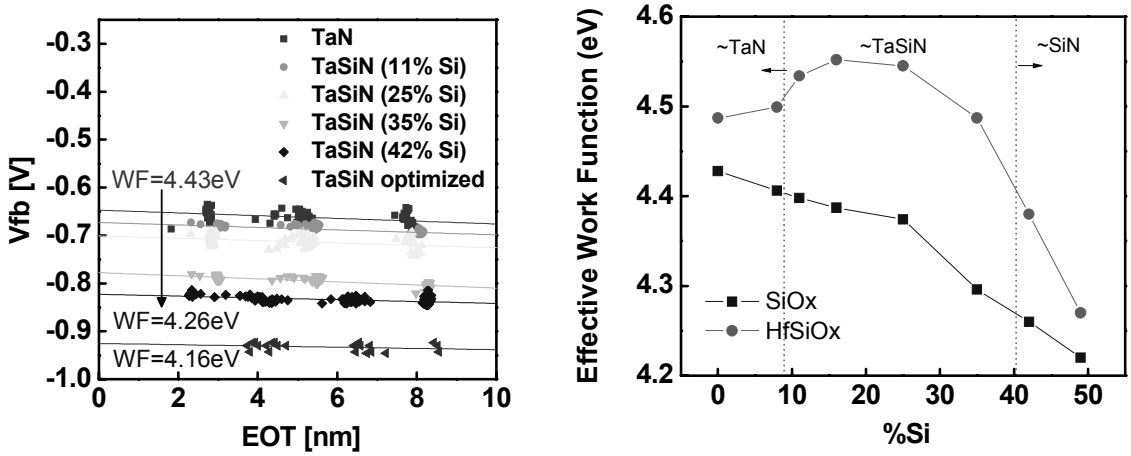


Figure 4.16 (a) V_{fb}-EOT plot of TaSiN on terraced oxide for work function extraction as a function of at% Si. (b) Effective work function of TaSiN on SiO_2 and $HfSiO_x$ as a function of at% Si.

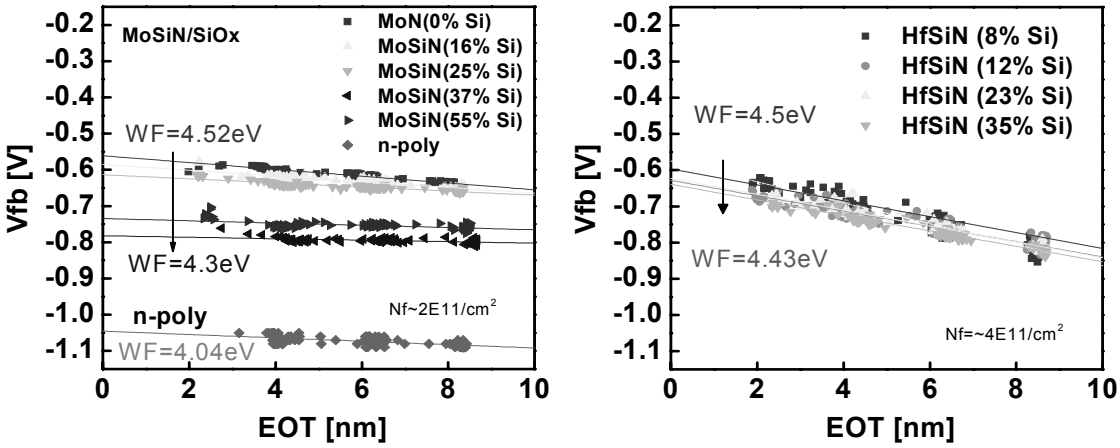


Figure 4.17 (a) V_{fb}-EOT plot of MoSiN on oxide for work function extraction as a function of at% Si and (b) HfSiN on terraced oxide with 40Å HfO_2 for work function extraction as a function of at% Si.

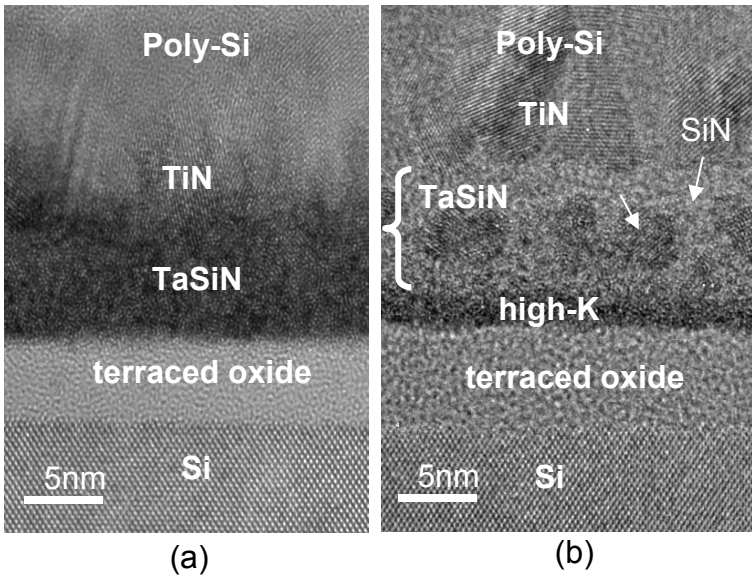


Figure 4.18 HRTEM image of the TaSiN metal gate on terraced oxide stacks for (a) Ta-rich versus (b) Si-rich film. Phase separation is observed in (b).

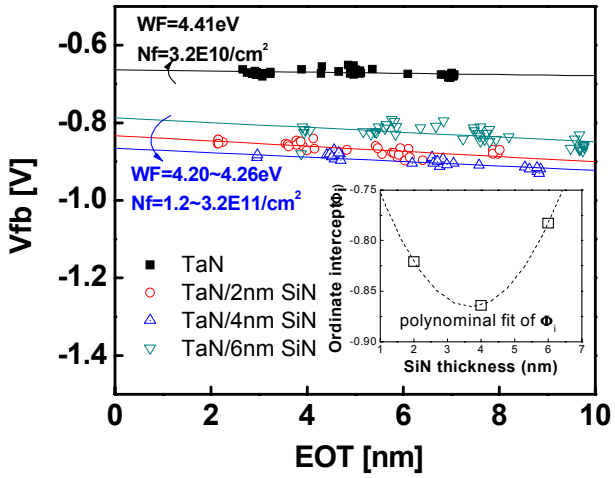


Figure 4.19 **V_{fb}-EOT plot of the TaN/SiN thickness series on terraced oxide. Insert plot is the ordinate intercept of V_{fb}-EOT versus SiN thickness, used for analysis of charge in dielectric stacks.**

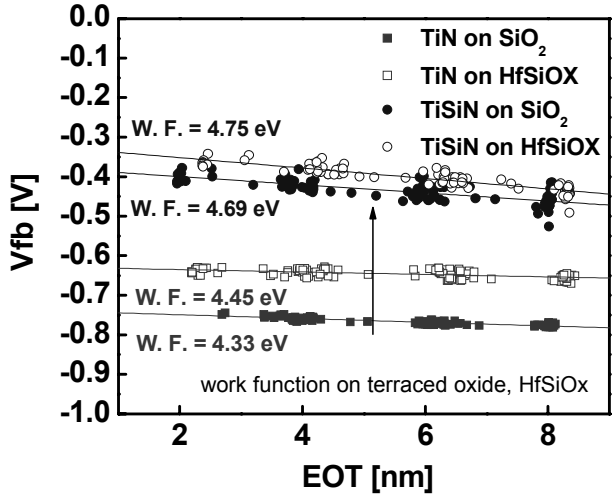


Figure 4.20 **Effective work function of TiN and TiSiN on SiO_2 and $HfSiO_x$.**

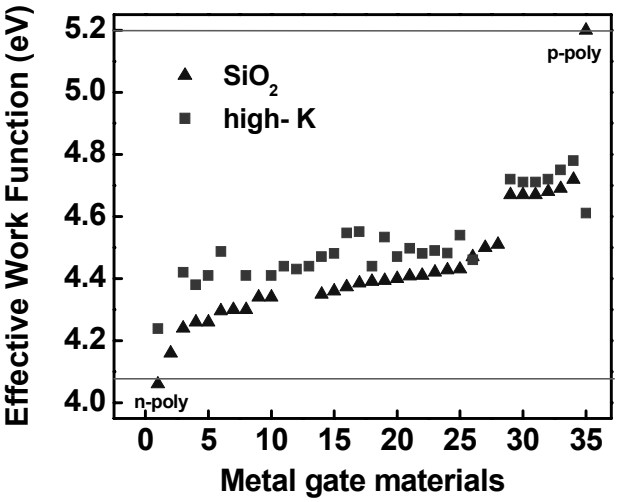


Figure 4.21 Summary of the effective work function of amorphous metal electrodes evaluated on SiO_2 & high-k.

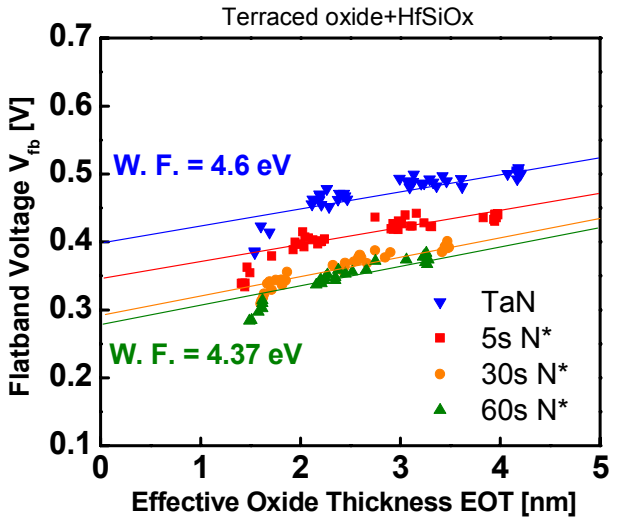


Figure 4.22 V_{fb}-EOT of a TaN/HfSiOx/terraced oxide stack, where the dielectric is exposed to various plasma nitridation times

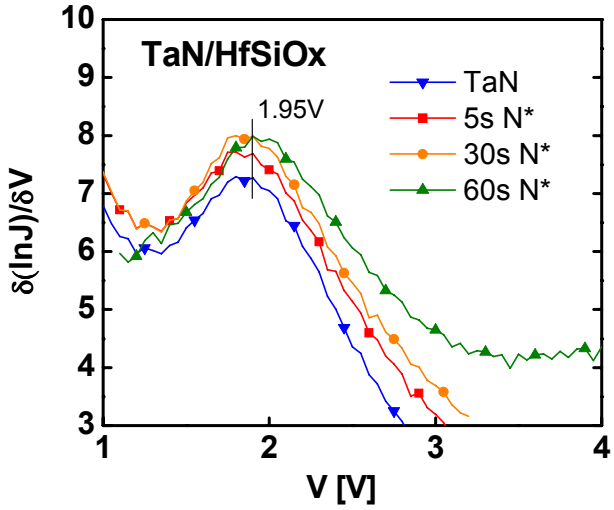


Figure 4.23 $\Delta\ln(J_g)/\Delta V_g$ relationship for metal/high-k barrier height extraction on TaN/HfSiOx/ terraced oxide stacks, where the dielectric is exposed to various plasma nitridation times

4.6 REFERENCES

[1] *Diagrammy Sostoianiia Metallicheskikh sistem, Moscow*, 1971.

[2] H. Michaelson, "The work function of the elements and its periodicity," *Journal of Applied Physics*, vol. 48, pp. 4729-4733, 1977.

[3] V. Misra, H. C. Zhong, and H. Lazar, "Electrical properties of Ru-based alloy gate electrodes for dual metal gate Si-CMOS," *Ieee Electron Device Letters*, vol. 23, pp. 354-356, 2002.

[4] H. C. Wen, K. Choi, P. Lysaght, P. Majhi, H. Alshareef, C. Huffman, R. Harris, H. Luan, B. H. Lee, N. Yamada, and S. Wickramanayaka, "Work function engineering of RuHf alloys as gate electrodes for future generation dual metal CMOS," presented at VLSI Technology, 2005. (VLSI-TSA-Tech). 2005 IEEE VLSI-TSA International Symposium on, 2005.

[5] J. K. Schaeffer, S. B. Samavedam, D. C. Gilmer, V. Dhandapani, P. J. Tobin, J. Mogab, B. Y. Nguyen, B. E. White, S. Dakshina-Murthy, R. S. Rai, Z. X. Jiang, R. Martin, M. V. Raymond, M. Zavala, L. B. La, J. A. Smith, R. Garcia, D. Roan, M. Kottke, and R. B. Gregory, "Physical and electrical properties of metal gate electrodes on HfO2 gate dielectrics," *Journal of Vacuum Science & Technology B*, vol. 21, pp. 11-17, 2003.

[6] H.-C. Wen, K. Choi, P. Majhi, H. Alshareef, C. Huffman, and B. H. Lee, "A systematic study of the influence of nitrogen in tuning the effective work function of nitrided metal gates," presented at VLSI Technology, 2005. (VLSI-TSA-Tech). 2005 IEEE VLSI-TSA International Symposium on, 2005.

[7] H. Y. Yu, M. F. Li, and D. L. Kwong, "Thermally robust HfN metal as a promising gate electrode for advanced MOS device applications," *Ieee Transactions on Electron Devices*, vol. 51, pp. 609-615, 2004.

[8] J. Westlinder, G. Sjoblom, and J. Olsson, "Variable work function in MOS capacitors utilizing nitrogen-controlled TiNx gate electrodes," *Microelectronic Engineering*, vol. 75, pp. 389-396, 2004.

[9] W. Gordy and W. J. O. Thomas, "Electronegativities of the Elements," *The Journal of Chemical Physics*, vol. 24, pp. 439-444, 1956.

[10] J. Schaeffer, D. Gilmer, S. Samavedam, D. Triyoso, R. Hegde, S. Kalpat, M. Raymond, C. Capasso, B. Taylor, M. Sadd, H. H. Tseng, M. Stoker, A. Haggag, D. Roan, L. L. Happ, C. , P. J. Tobin, and B. E. White, "Materials Challenges for High Permittivity Gate Dielectrics and Metal Gate Electrodes," *IEEE ISAGST 2006*, 2006.

[11] M.-A. Nicolet and P. H. Giauque, "Highly metastable amorphous or near-amorphous ternary films (mictamict alloys)," *Microelectronic Engineering*, vol. 55, pp. 357-367, 2001.

[12] Y. S. Suh, G. P. Heuss, J. H. Lee, and V. Misra, "Effect of the composition on the electrical properties of TaSixNy metal gate electrodes," *Ieee Electron Device Letters*, vol. 24, pp. 439-441, 2003.

[13] T. Hori, *Gate dielectrics and MOS ULSIs: Principles, Technologies and Applications*. Germany: Springer.

[14] R. Lin, Q. Lu, P. Ranade, T. J. King, and C. M. Hu, "An adjustable work function technology using Mo gate for CMOS devices," *Ieee Electron Device Letters*, vol. 23, pp. 49-51, 2002.

CHAPTER 5

MODULATION OF METAL/HIGH-K STACK INTERFACE FOR EWF TUNING

5.1 INTRODUCTION

Based on our systematic study of metal EWF in Chapter 4, the range of EWF tunability achieved for thermally stable metal electrodes is found to be limited to ~4.2~4.9eV. Therefore, engineering of the interface structure between the metal/dielectric to tune the EWF of metals becomes more feasible, compared to changing the materialistic characteristic of the bulk metal film. Two methods of interface engineering to obtain band-edge EWF are discussed in this Chapter. One such technique is via insertion of a dielectric layer between the metal/high-k dielectric. The other is the utilization of interfacial diffusion/reaction between the metal/dielectric to form an desired interface structure. The mechanisms for the EWF control is discussed, and some transistor device results are shown.

5.2 IMPACT OF INTERFACIAL ENGINEERING ON EWF: INTERFACE ENGINEERING TOWARD P-TYPE BAND EDGE

For engineering toward p-type EWF, an Al-based top interface layer (TIL) such as ALD Al_2O_3 or PVD AlO_x, or AlN of ~1nm is used. This phenomenon has been utilized in memory application [1], but threshold voltage tuning using band offset engineering is a new approach. Figure 5.1 shows the schematic of the gatestack with the TIL. EWF of the stacks were evaluated with the terraced oxide structures after 1000^{o}C thermal budget. For stacks with additional Al_2O_3 TIL capping, the EWF values of metal

electrodes increased by ~250±50 meV from their initial values(Figure 5.2(a)). Figure 5.2(b) shows the similar shift with the Al_2O_3 TIL (and AlN stacks) independent of the metal electrode system. There have been previous reports on the EWF shift by Al containing high-k dielectrics [2, 3]. However, the physical mechanism behind such EWF shift has not been fully investigated and mainly attributed to negative charge within AlO_x layer or Al diffusion into interfacial oxide or silicon [2,3]. Since the V_{fb} change in Figure 5.2(a), is independent of EOT, there can be two main sources for the constant V_{fb} (EWF) change: 1) Similar to common explanations, the V_{fb} shift can be due to negative charges induced by the AlO_x TIL; 2) The second source of a constant V_{fb} shift can be due to a fixed dipole formation within the gatestack.

5.2.1 Possibility of negative charge on V_{fb} shift

First to address the possibility of negative charges causing the V_{fb} shifts. Sources of the charge can be from a) Al_2O_3 bulk charge, b) charge (Q_{HfO-Al}) formed by Al diffusion into the dielectric, c) interface charge formed at the high-k/AlO interface or d) below the high-k at the SiO_2 (Q_{HfO_SiO})or Si interface due to Al diffusion. Figure 5.3 is the schematic showing location of such charges with in the dielectric stack. Thickness series of Al_2O_3 (2, 4, 6 and 8nm) were deposited on terraced oxide dielectrics for bulk charge density calculations. The V_{fb}-EOT relationship for the various Al_2O_3 thickness are shown in Figure 5.4. Utilizing the V_{fb} equation based in Chapter 2, we are able to estimate the bulk charge density for Al_2O_3 to be ~-7E18/cm^3. Thus, for a 1nm Al_2O_3 film, the bulk charge contribution on the V_{fb} is <20meV, and cannot explain the ~300meV V_{fb} shift with Al TIL (not charge from Figure 5.3-a). Temperature dependent studies of the Al_2O_3/$HfSiO_x$ stack EWF, shows no EWF increase for samples just after a FG anneal, while increased EWF is observed only after 700~1000^{o}C (Figure 5.5). The same EWF

observed for the Al_2O_3 sample after FG anneal, and the no TIL control, also suggests minimal impact of Al_2O_3 bulk charge on V_{fb}. Secondary ion mass spectroscopy (SIMS) profile comparison of the sample after FG anneal, 700°C, and 900°C show Al diffusion into the high-k layer after anneal. The diffusion of Al is limited to the high-k/SiO_2 interface (700°C), and is not enhanced with additional annealing (900°C), but higher temperature causes the Al profile to redistribute toward the electrode. Interestingly, the EWF for the annealed samples are constant even up to 1000°C, suggesting the charges caused by Al diffusion into the high-k (charge from Figure 5.3-b) may not be the source of the V_{fb} shift from the TIL. If charges are located at the high-k/SiO_2 interface (Figure 5.3-c), there should be a linear dependence in the V_{fb} change with the distance to the electrode (x):

$$\Delta V_{FB} = -\frac{Q_{HfO\_SiO}}{\varepsilon_h} x$$

Therefore, an experiment with a TIL on varied high-k thickness (2.5, 3.5, 4.5 and 6.5nm HfSiOx) on terraced oxide has been conducted to change the distance of the charge frm the electrode (x) (Figure 5.7). A constant ~240meV difference is observed with the TIL independent of the high-k thickness, suggesting the charge at location c) is not responsible for the V_{fb} change. SIMS analysis of the 65Å $HfSiO_x$ stack also shows Al distribution throughout the high-k dielectric. However, limited Al diffusion is observed through SiO_2, with no detectable Al is observed at the Si/SiO_2 interface (Figure 5.8). Also, since the V_{fb} change is independent on the terraced oxide band thickness, this supports charge at the Si/SiO_2 interface (d) is also not the source of V_{fb} shift.

5.2.1 Possibility of dipole on V_{fb} shift

The other possibility for such constant V_{fb} shift would be explained by a dipole formation in the dielectric stack. An electric dipole is a separation of positive and

negative charge. Figure 5.9 is a schematic showing the formation of a dipole within the dielectric due to charge **q**, its effect on the V_{fb} is shown in the equation below:

$$\Delta V_{FB} = -\frac{q(x+d)}{\varepsilon_{ox}} + \frac{q \cdot x}{\varepsilon_{ox}} = -\frac{q \cdot d}{\varepsilon_{ox}}$$

Figure 5.9 also shows the possible dipole locations within the stack, this includes a) interface dipole formation between metal/high-k; similar to Fermi-level pinning, b) interface dipole formation at Al_2O_3/high-k interface, c) SiO_2/high-k interface, and d) remote interaction between the high-k/Si. Since nearly constant EWF shift is observed for several metals covering a wide range of EWF (4.2~4.8 eV), change in the interface dipole at the metal/dielectric interface may not explain these shifts. To determine which interface is the effective dipole location, a complementary set of samples to modulate Al distribution in the gate stack is processed. (Figure 5.10). Since dipole formation may be a thermally activated process, direct comparison of the stacks after an equal high thermal budget (1000^{o}C) is needed. Set (A) is the baseline AlO/HfO stack. In the as-deposited low thermal budget state, the EWF of the stack is similar to the without TIL as shown in Figure 5.5 (4.75eV). With process changes in the high-k (with and without high-k post deposition anneal (PDA)), we can control the Al-diffusion profile to two forms. First, even after a 1000^{o}C anneal, the Al profile however is limited, and the top dielectric surface is Al-rich (Figure 5.11 (a)). This sample exhibits an EWF similar to the without TIL control (4.8eV) (Figure 5.12), suggesting the AlO/high-k interface dipole (Figure 5.9-b), and the metal/AlOx interface dipole (Figure 5.9-a) is not effective in changing V_{fb}. Second, an uniform distribution of Al toward the high-k/SiO_2 interface is obtained if the high-k does not have a PDA (Figure 5.11 (b)). Here, allowing Al diffusion to the SiO_2 interface exhibits the V_{fb} increase effect (EWF=5.05eV) (Figure 5.12). This is consistent with the temperature dependence in EWF, where high EWF is only observed when Al

diffuses to the SiO_2 interface (Figure 5.6). Set (B) HfO/AlO in Figure 5.10 is the reversed stack of (A), with direct deposition of AlO_x on SiO_2, and represents intentional Al incorporation at the SiO_2 interface. This sample exhibits equal EWF as the AlO/HfO stack (5.05eV), and would support the concept of dipole formation at the high-k/SiO_2 interface (Figure 5.9-c).

Based on these analysis, previous reports of Al containing dielectrics exhibiting a characteristic negative charge at the Si interface [4, 5] could be interpreted by the formation of a dipole layer between Al-dielectrics and the inevitable bottom interfacial oxide layer. A schematic of how interface dipole formation will shift the band offset and result in increased EWF is shown in Figure 5.13. Origin of the possible mechanisms for the dipole may be the formation of Al-O bonds at the interface, or the high reactivity of Al with SiO_2. Figure 5.14 shows the Al 2*p* and Si 2*p* binding energies before and after anneal at 1000 °C, 5 s in N_2. Note that there is a chemical shift in the Al 2*p* binding energy after the anneal indicative of Al–O bond formation, and a shift in the Si 2*p* binding energy indicative of sub-oxide formation (SiO_x) [6]. This result suggests Al in the AlN*x* layer may reduce the Si–O bonds in the gate dielectric, resulting in Al–O bond formation at the AlN*x* /SiO_2 interface. Such a reaction is thermodynamically favorable since the free energies of formation, for Al_2O_3, SiO_2, and AlN*x* are −1582, −853, −287 kJ/mol, respectively.

5.3 INTERFACE MODULATION VIA BULK METAL ELECTRODES

Al-based metal electrodes for p-type band edge metal: Metal-Aluminum-Nitride

Use of an AlO_x or AlN capping layer on high-k dielectrics has been proposed as an effective method for modulating the effective work function toward the p-type band edge (Section [6-8]). However, the effective oxide thickness (EOT) increases ~1-2Å with these dielectric capping layers. To utilize the advantage of maintaining an Al-like interface between the high-k and metal electrode, interest has focused on incorporating Al in the electrode. TiAlN [9]and TaAlN [10] have been proposed to exhibit a 5.0eV EWF on SiO_2, however EWF on high-k is limited to less than 4.8eV. Based on the learning in Section 5.2, the key to high EWF is to allow Al diffusion for engineering at the high-k/SiO_2 interface. This study includes a systematic EWF evaluation of M-Al-N, M=Mo, W and Ru, to increase the starting metal EWF, targeting near band-edge p-type EWF of 4.9~5.1eV on high-k dielectrics.

Figure 5.15 is the phase diagram for MoAlN [11]. No ternary phase is observed for these M-Al-N systems, however, a tie line exists between the MoN and AlN phase. The MoAlN film deposited by PVD targets compositions along this tie line. Figure 5.16 is the EWF extracted from the V_{fb}-EOT relationship on terraced oxide structures. Consistent with that observed in Al TIL stacks, an EWF increase of ~200meV is observed for several MAlN systems compared to their MN_x counterparts. The parallel shift in the V_{fb}-EOT relationship suggests a constant fixed oxide charge and minimum effect on the interface with Al incorporation. An EWF as high as 5.08eV can be obtained with RuAlN systems. A systematic study of the EWF as a function of Al sputtering power is shown in

Figure 5.17. The addition of Al is shown to increase the EWF for a series of MAlN (M=Ta, Ti, Mo, W) and saturates as atomic % if Al is >15%. The metal/dielectric

barrier height was measured using the current derivative technique [12], where the voltage at the peak of the current derivative corresponds to the metal/dielectric barrier height (Figure 5.18(a)). The TaN and WN controls exhibit a 2V and 2.1V peak, respectively, and the addition of the electron affinity for $HfSiO_x$ (2.6eV [13]) equals 4.6eV, 4.7eV, which correlates to the EWF extracted from the terraced oxide. An increase in the barrier height (2.4V) is observed for WAlN, which is consistent with the change in the bulk WF of the electrode, as well as the formation of an interface dipole at the metal/high-k interface. Careful examination of the film properties by X-ray diffraction (XRD) shows the film is crystalline and composed of mainly Mo_2N with possible AlN phases after a 900^{o}C thermal budget, thus the change in bulk work function may not be able to completely explain the EWF differences (Figure 5.18(b)). The mechanism for the EWF increase is found to be consistent with that of AlO_x TIL. Figure 5.19 shows the temperature dependence of the EWF. Only the samples after annealing, where the interfacial Al distributes to the dielectric (confirmed by SIMS), will exhibit the EWF increase.

Demonstration of MAlN transistor devices shows that compared with TiSiN electrodes with an AlO_x interface layer, a comparable V_{fb} is achieved with no evident EOT increase. Therefore, an Al-containing metal is a more favorable approach for interface modulations compared to the TIL approach (Figure 5.20). Comparable device performance is maintained with MoAlN exhibiting mobility ~96% of its control TaN electrode (Figure 5.21(a)). A slight degradation in the interface state density measured by charge pumping technique (Figure 5.21(b)), could be the source of the degraded mobility. The increased interface states would be consistent with Al interaction with the SiO_2 interface layer. Threshold voltage can be reduced ~0.2eV with MoAlN electrodes; however, it still is 150meV higher than that expected from an 4.95eV work function

electrode (Figure 5.22). This is believed to be due to a newly identified V_{fb} roll-off effect commonly observed in high work function electrodes as devices scale to lower EOTs. More discussion of this new phenomena will be discussed in the Chapter 7. Nevertheless, interface engineering is identified to be feasible technique for EWF control with good device performance.

5.4 INTERFACE ENGINEERING TOWARD N-TYPE EWF

With a similar approach, the insertion of an interfacial layer to engineer the interface toward n-type EWF is shown with the use of La_2O_3 dielectrics (Figure 5.23)[14]. The La_2O_3 film thickness are 0.5 and 1.0 nm thick interlayers. These thickness values result, upon mixing of the two dielectrics after a thermal budget, and results in a dielectric layer with 15 and 28 atomic % La, respectively. Figure 5.24 shows a backside SIMS depth profile of the gate stack after La_2O_3 deposition and annealing at 1070 °C spike anneal. The results show that La and Hf signal overlap, indicating that the La has completely mixed with the $HfSiO_x$ gate dielectric after device fabrication. The transistor CV curves for devices with HfSiO film and for devices with HfLaSiO dielectric formed using the La_2O_3 capping process indicate a distinct shift in the V_{fb} and V_t of the devices with increasing La_2O_3 content (Figure 5.25). Notice that the CV curves are shifted in parallel without any stretch or distortion in the transistor CV curves. The threshold voltage shifted by nearly 400 mV with the initial addition of about 15% La (0.5 nm La_2O_3 capping layer) and another 550mV with the addition of 28% La (1.0 nm capping layer) (Figure 5.26). In fact the V_t of the device with 1.0 nm La_2O_3 capping is the same as that of our reference n+ poly-Si using the same transistor fabrication flow (0.27 V). The significant reduction in V_t actually takes place without compromising the EOT of the stack. Figure 5.27(a) shows the high field mobility of the gate stack is not

degraded by the incorporation of the La_2O_3 capping layer and that mobilities as high as 92% of the universal SiO_2 curve can be achieved. However, the low-field mobility is somewhat degraded, with the degradation amount being dependent on the amount of La_2O_3 added. Pulsed I_d-V_g technique is applied to investigate the degree of dielectric charge trapping with the addition of La doping, and no significant increase is observed. Concurrently, it is unlikely that all La_2O_3 remains on top of the dielectric. La_2O_3 is one of the most aggressive silicate formers in the lanthanide series [15]and therefore La may seek out the interfacial SiO_x to form La silicate [16]. Peak mobility loss (Figure 5.27) may be due to coulomb scattering from La near the IL SiO_x.

The mechanism by which the work function shift may occur may be related to either bulk or interfacial phenomenon. One possibility is that La-related bulk positive charges in the $HfSiO_x$ dielectric shift the C-V curve to lower (more negative V_{fb}) values and hence lower NMOSFET V_t. Support for this hypothesis comes from the La_2O_3 thickness dependence of the V_t shift (Figure 5.26) and also from the low-field mobility degradation shown in Figure 5.27. However, La-related bulk charges cannot *alone* entirely account for the entire V_{fb} shifts. An alternative explanation, consistent with other reports [17, 18], is that electropositive La forms a La-O dipole at the high-k interface that shifts the band offset and therefore the EWF of the metal. Yamamoto et al. has reported a systematic comparison of HfLaO stacks with various La concentrations similar to that we have done for the Al stack, and also believes the location for the dipole is located at the high-k/SiO_2 interface [19]. Concurrently, the interface engineering technique can also be applied for other Lanthanide doped metal gates and exhibit near n-type band edge EWF.

5.5 SUMMARY

Control of the EWF by interface engineering is found to be a viable approach for tuning thermally stable metal electrode systems toward band-edge without compromising device performance. Since the key modulations are located at the high-k/SiO_2 interface, it suggests a broad process flexibility, independent on bulk electrode material properties, and would be applicable to variety of metal gate systems.

5.6 FIGURES

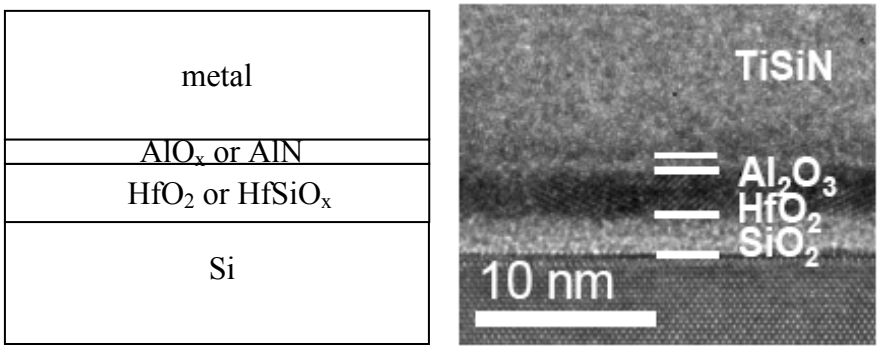
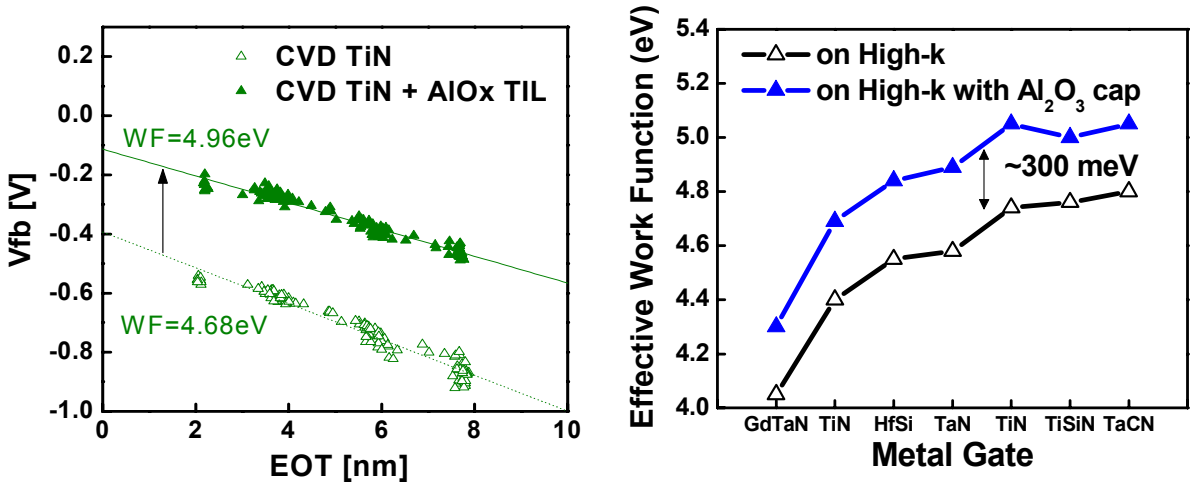


Figure 5.1 Schematic of the Al-based TIL on high-k. Actual HRTEM image of the metal/Al_2O_3/HfO_2 stack included on the right.



(a) (b)

Figure 5.2 (a) V_{fb}-EOT plot for CVD TiN electrode with and without a AlO_x TIL. (b) EWF for various metal electrode systems showing the TIL results in a constant increase in EWF~300meV.

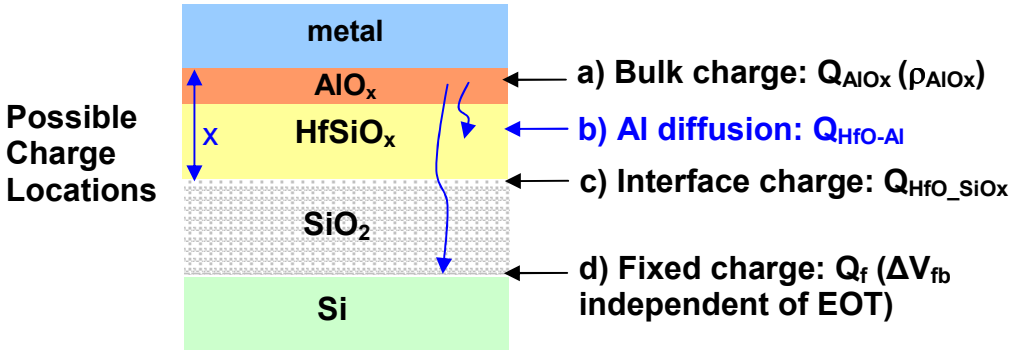
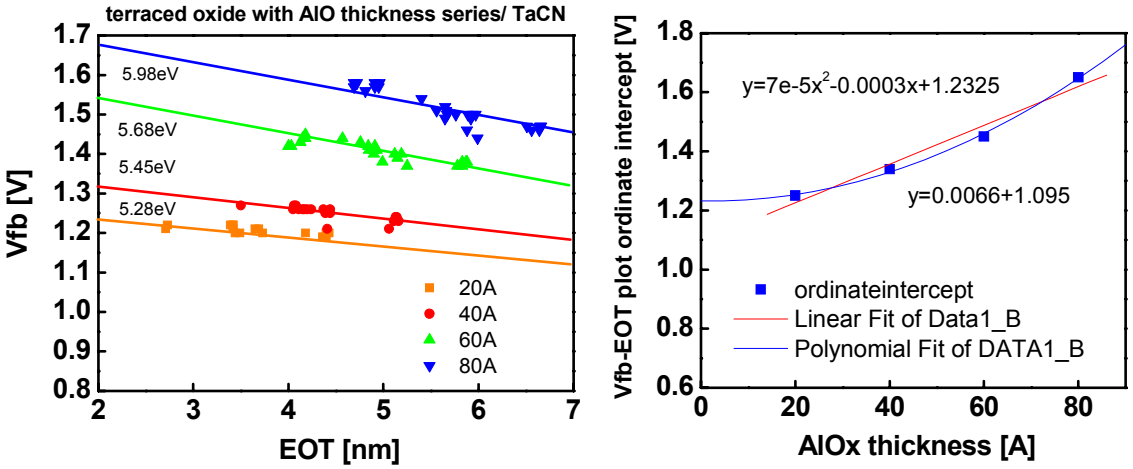


Figure 5.3 Schematic of possible charge locations in the AlO_x TIL/high-k stack



(a) (b)

Figure 5.4 **(a)V_{fb}-EOT plot for Al_2O_3 thickness series (20, 40, 60, 80Å) on terraced oxide (b) Plotting the y-ordinate intercept from plot (a) against Al_2O_3 film thickness can extract the bulk and interface charge between Al_2O_3 and SiO_2.**

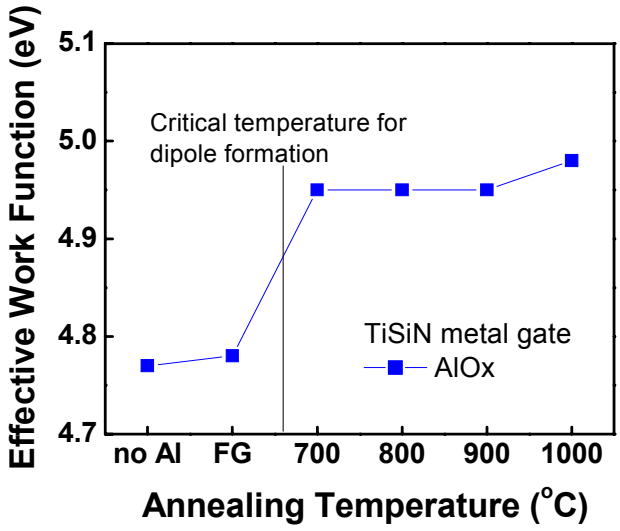


Figure 5.5 **Temperature dependence of EWF for TiSiN metal electrode with AlOx TIL capping on high-k.**

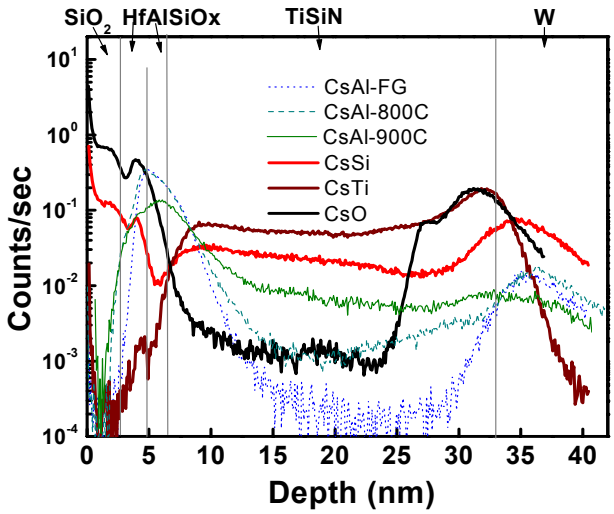


Figure 5.6 **Secondary ion mass spectroscopy profiles of the TiSiN/AlO_x/$HfSiO_x$ stack after FG, 700°C and 900°C annealing, showing the Al redistribution and diffusion into the high-k.**

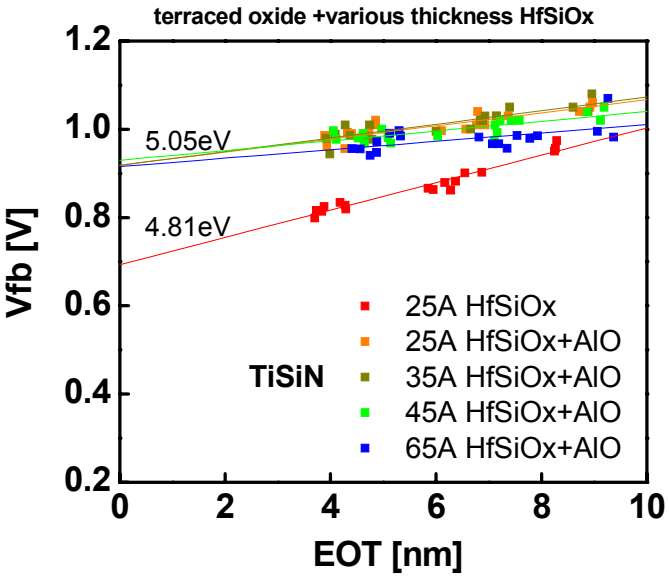


Figure 5.7 **V_{fb}-EOT plot for EWF extraction of thickness series of high-k ($HfSiO_x$) with AlO_x TIL on terraced oxide.**

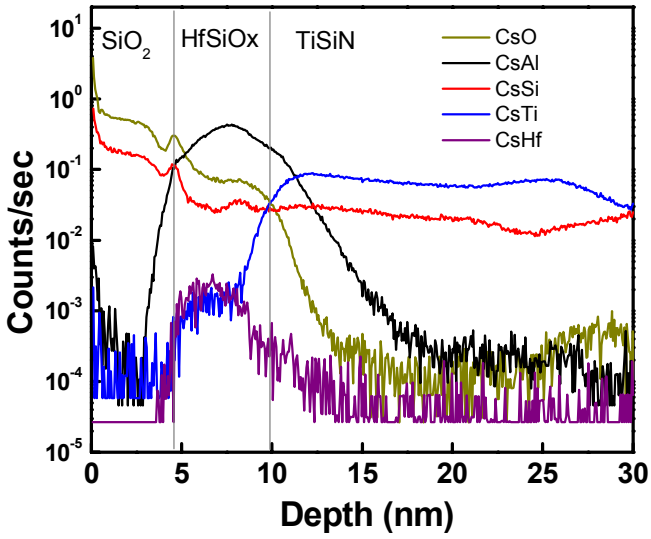


Figure 5.8 **Backside SIMS of the 65Å HfSiOx with AlO TIL on terraced oxide to show the Al distribution after annealing.**

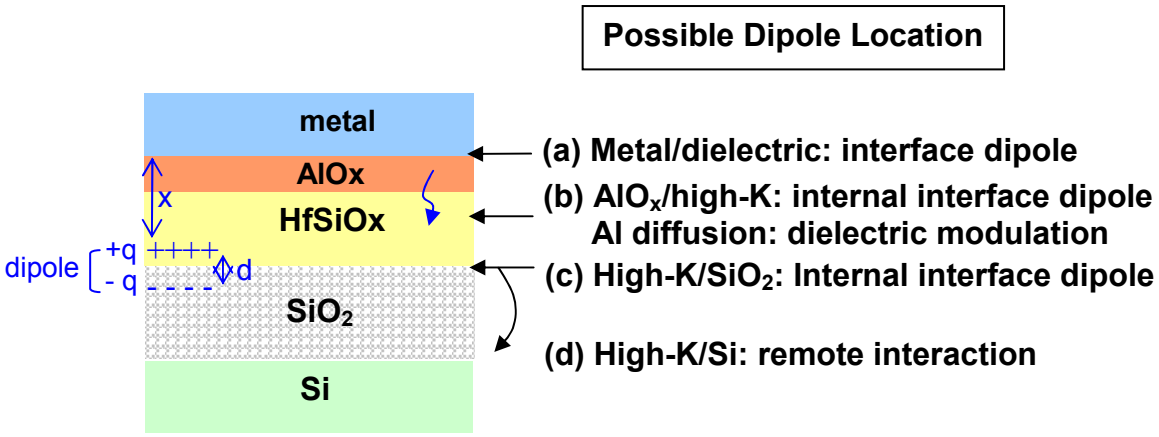


Figure 5.9 **Schematic showing possible dipole locations within the gatestack due to use of AlO TIL.**

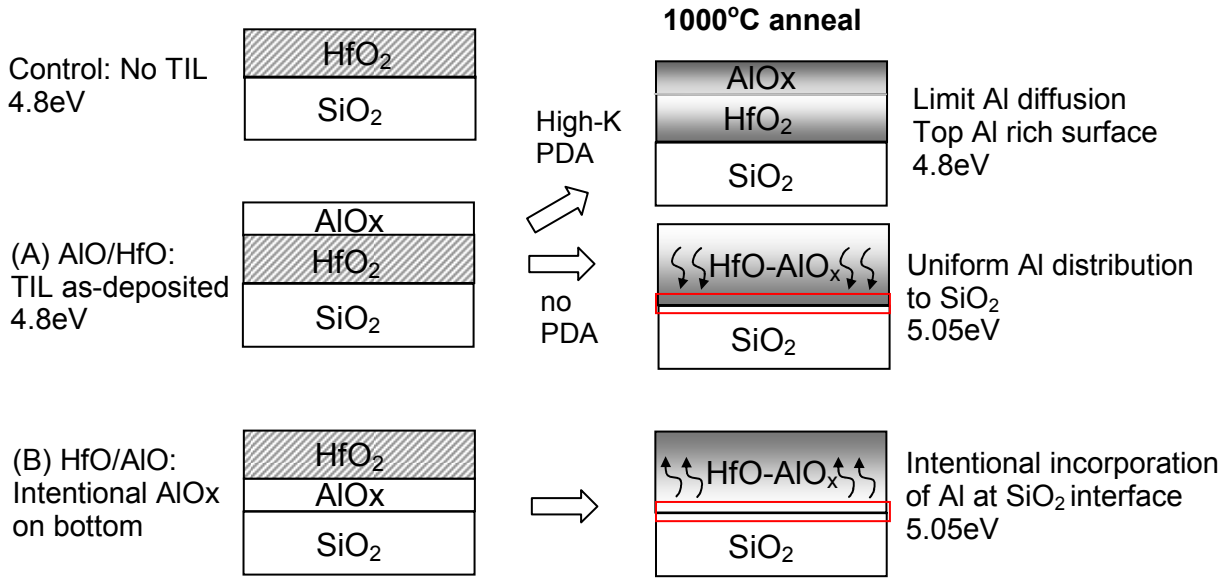


Figure 5.10 **Schematic of experiment set conducted to verify dipole location. Set (A) AlO TIL on HfO_2 as-deposited, and after 1000°C annealing; with varied high-k PDA processes. Set (B) Reverse AlO TIL below HfO_2 as deposited and after 1000°C annealing**

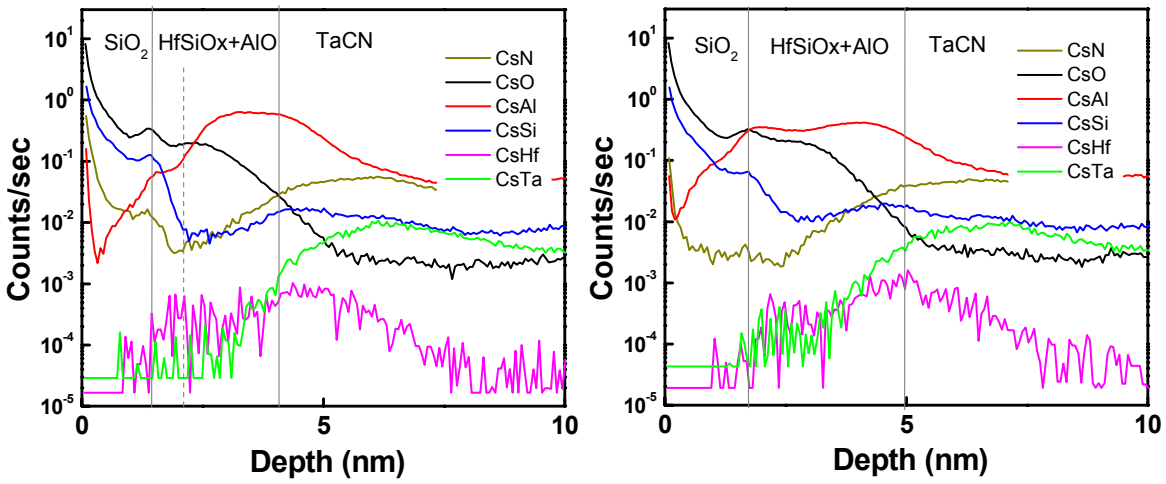


Figure 5.11 Backside SIMS profile showing the AlO TIL/HfO_2 stacks after 1000°C with (a) Al rich top interface and (b) uniform Al distribution in the dielectric.

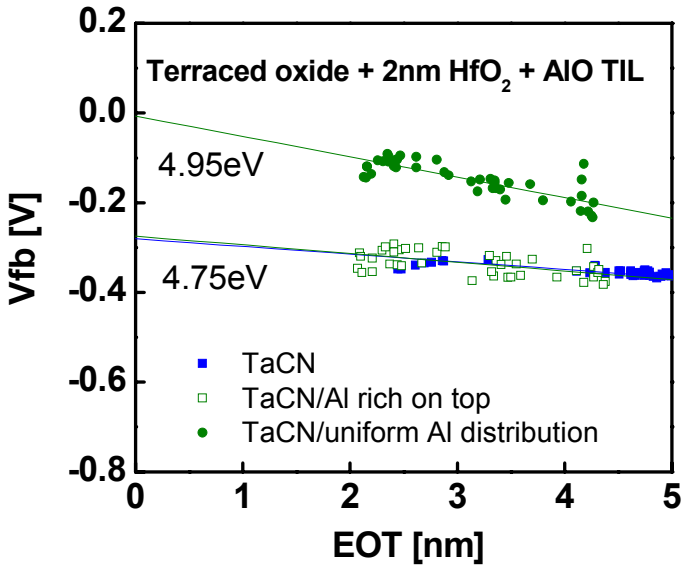


Figure 5.12 V_{fb}-EOT plot showing EWF for the AlO TIL/HfO_2 stacks with varied Al distribution

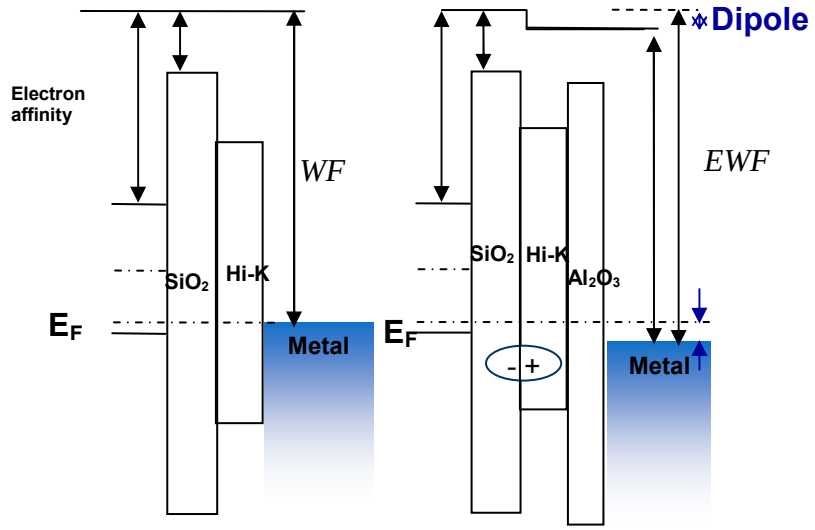


Figure 5.13 Schematic showing the effect of a dipole on the band diagram at for example the AlO TIL/high-k interface

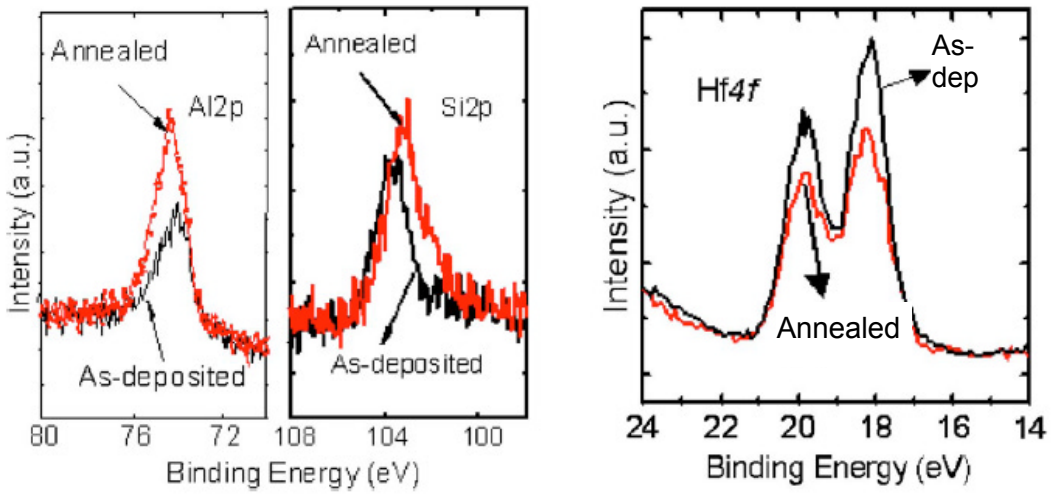


Figure 5.14 XPS analysis of the AlO/SiO_2 stack before and after anneal, showing the reduction of SiO_2 from Al after annealing. No significant change in the Hf 4f peak location is observed suggesting minimum modulation in the high-k dielectric from Al incorporation [6].

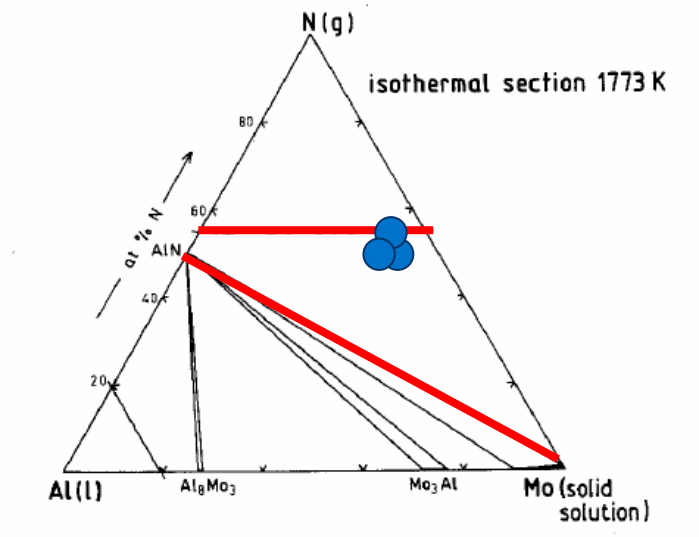


Figure 5.15 **Phase diagram for MoAlN. Film compositions investigated in this study are highlighted.**

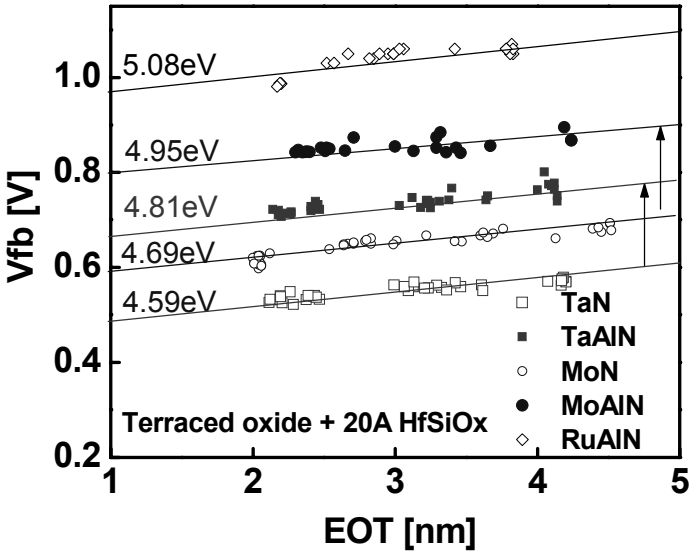


Figure 5.16 **V_{fb}-EOT for EWF extraction for MN and MAlN.**

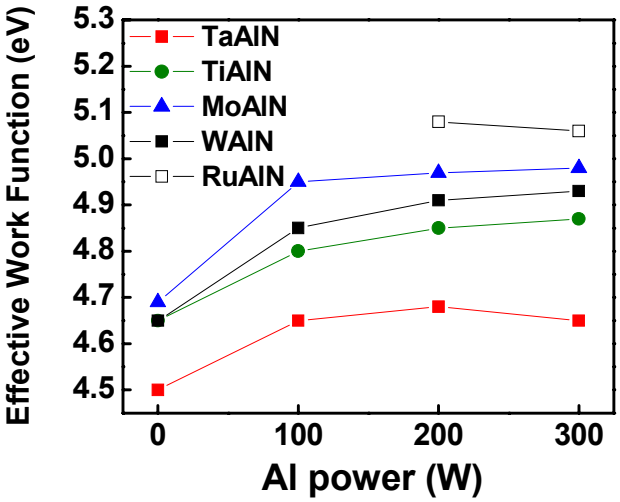


Figure 5.17 **EWF extraction for MAlN as function of Al sputtering power.**

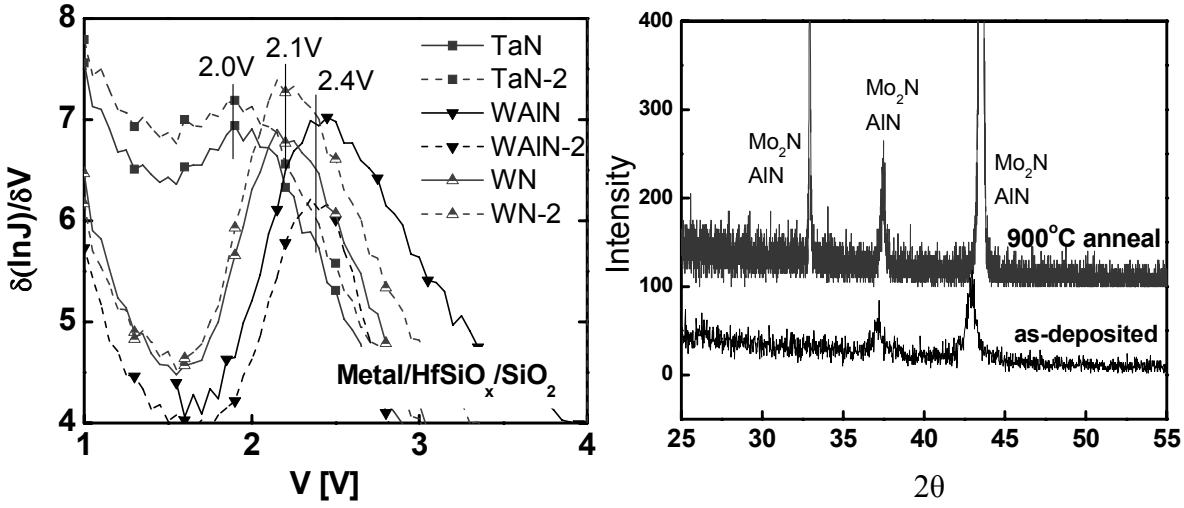


Figure 5.18 **(a) Metal/high-k barrier height measurements from peak of current derivative (b) XRD pattern for MoAlN before and after anneal.**

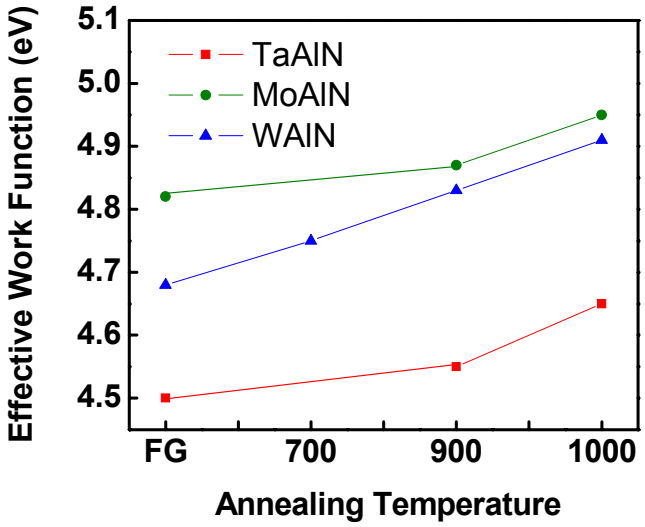


Figure 5.19 **Temperature dependence of the EWF for various MAlN.**

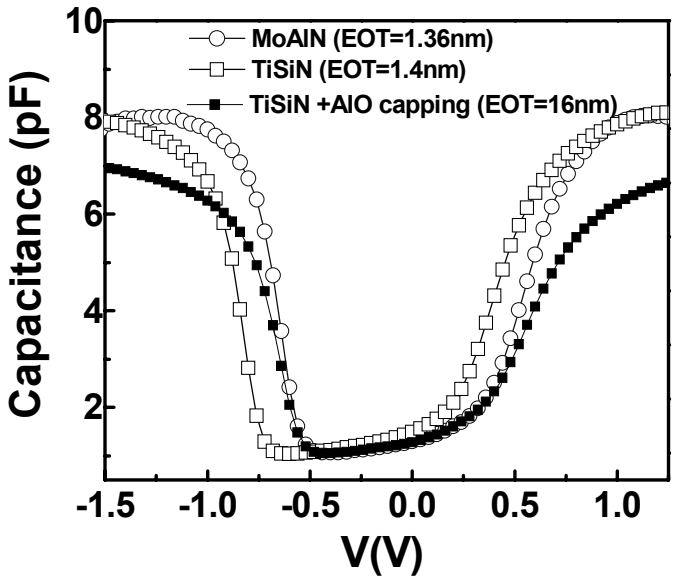


Figure 5.20 **Transistor CV for MoAlN compared to TiSiN and TiSiN+AlO interface layer**

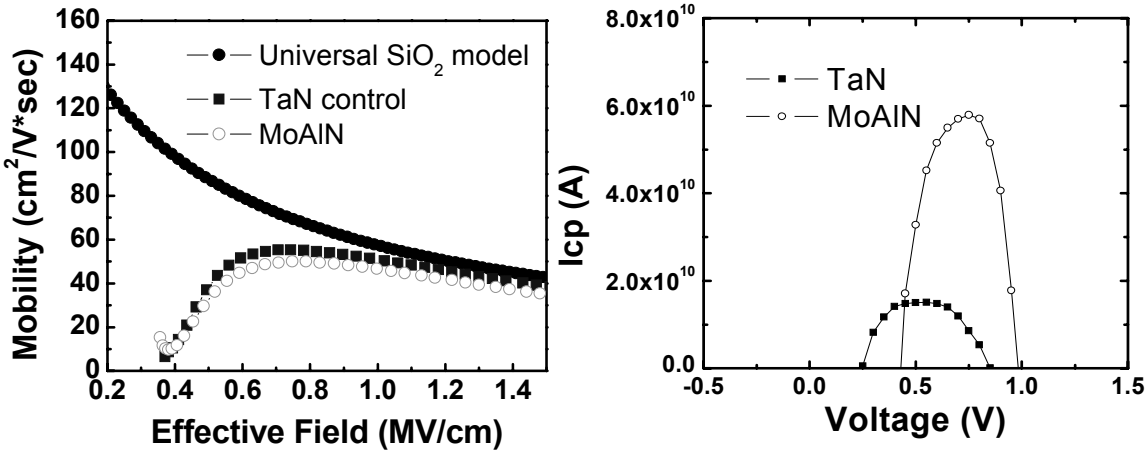


Figure 5.21 (a) Hole mobility for transistors with MoAlN compared to TaN electrode control, with slight degradation. (b) Interface state density measured by charge pumping.

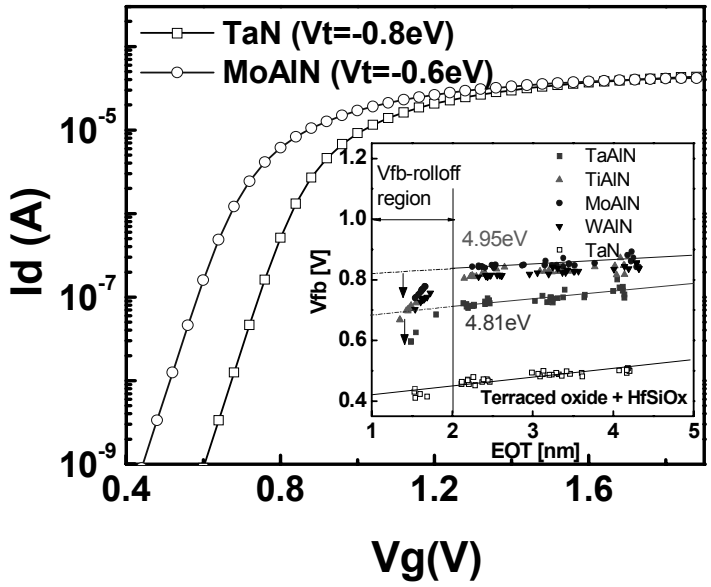


Figure 5.22 Transistor I_dV_g for MoAlN compared to TaN electrode.. Insert shows the V_{fb}-EOT rolloff behavior for MAlN.

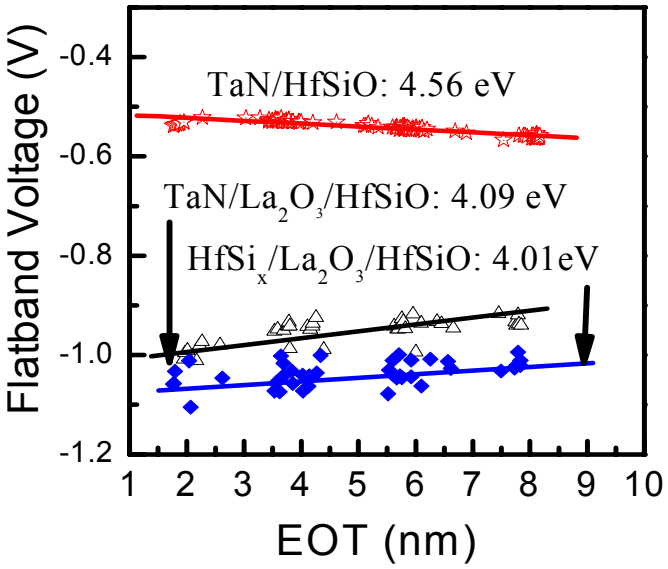


Figure 5.23 **V_{fb}-EOT plot for EWF extraction of various metals on high-k with an La_2O_3 TIL.**

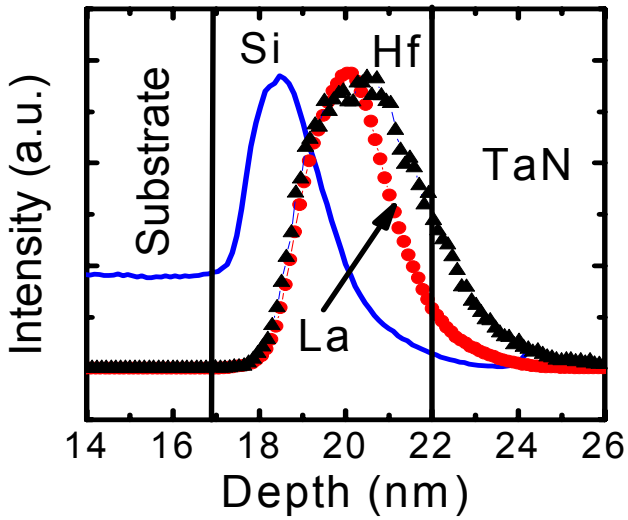


Figure 5.24 **Backside SIMS profile of the gate stack showing distribution of La into the high-k dielectric after anneal.**

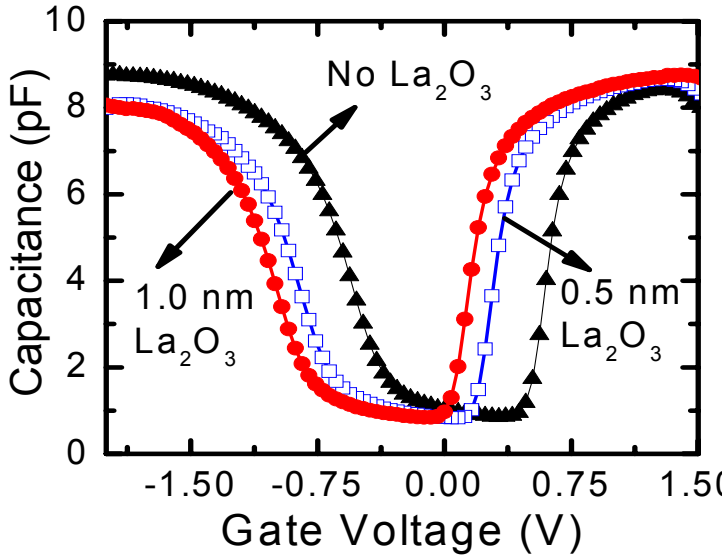


Figure 5.25 Transistor CV for samples with and without La_2O_3 TIL, and the thickness dependence of V_{fb} with the TIL thickness.

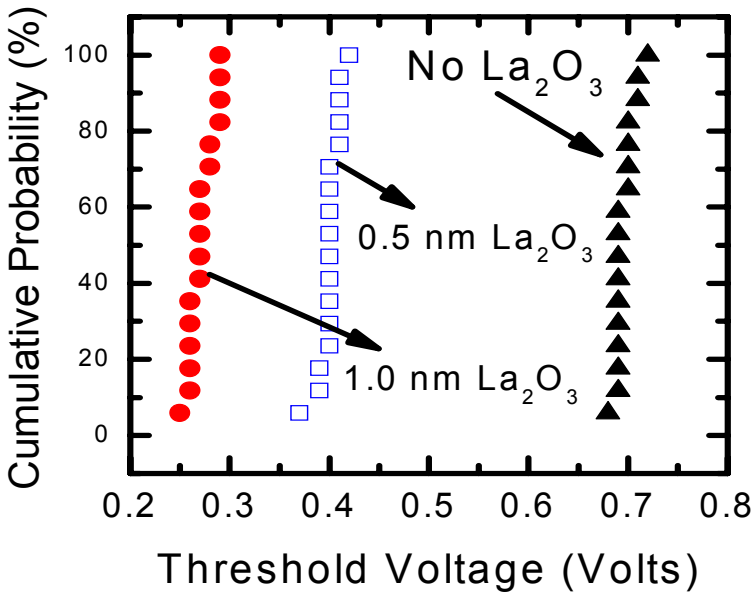


Figure 5.26 Transistor threshold voltage distribution samples with and without La_2O_3 TIL, and the thickness dependence of V_t with the TIL thickness.

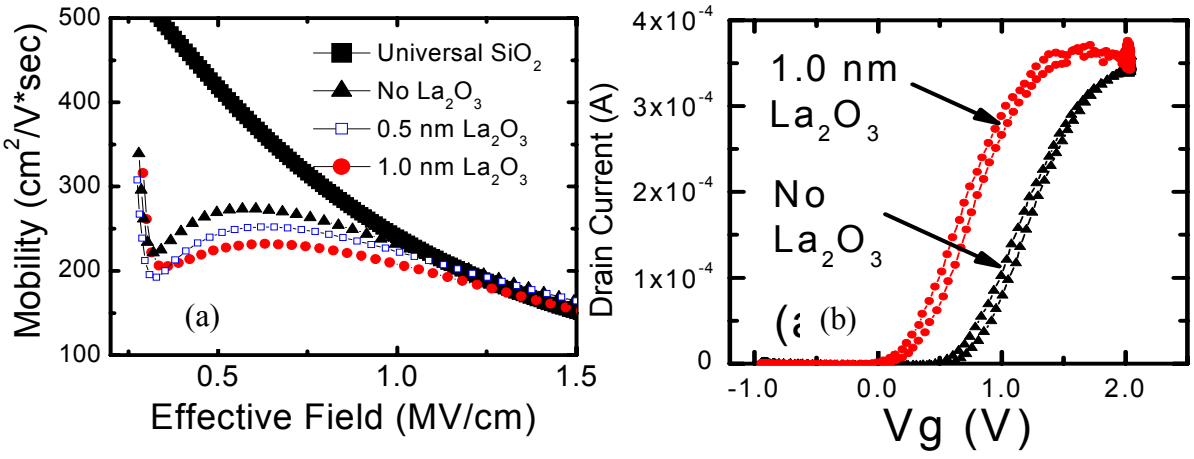


Figure 5.27 **Electron mobility plot versus effective field compared to the universal SiO_2 for samples with and without La_2O_3 TIL, and the thickness dependence in mobility with the TIL thickness. (b) I_d-V_g plot measured from the single pulse I_d-V_g technique with 5μs rise and fall time, and a 100 μs pulse width showing no significant charge trapping with La_2O_3 TIL compared to the control sample.**

5.7 REFERENCES

[1] W.-H. Lee, J. T. Clemens, R. C. Keller, and L. Manchanda, "A Novel High K Inter-poly Dielectric(IPD), A1/sub 2/O/sub 3/ For Low Voltage/high Speed Flash memories: erasing in msecs at 3.3V," presented at VLSI Technology, 1997. Digest of Technical Papers., 1997 Symposium on, 1997.

[2] S. B. Samavedam, L. B. La, P. J. Tobin, B. White, C. Hobbs, L. R. C. Fonseca, A. A. Demkov, J. Schaeffer, E. Luckowski, A. Martinez, M. Raymond, D. Triyoso, D. Roan, V. Dhandapani, R. Garcia, S. G. H. Anderson, K. Moore, H. H. Tseng, C. Capasso, O. Adetutu, D. C. Gilmer, W. J. Taylor, R. Hegde, and J. Grant, "Fermi level pinning with sub-monolayer MeOx and metal gates [MOSFETs]," *Electron Devices Meeting, 2003. IEDM '03 Technical Digest. IEEE International*, pp. 13.1.1-13.1.4, 2003.

[3] W. S. Yang, Y. K. Kim, S. U. Yang, J. H. Choi, H. S. Park, S. I. Lee, and J. B. Yoo, "Effect of SiO2 inermediate on Al2O3 and SiO2 n-poly Si interface deposited using atomic layer deposition (ALD) for deep submicron device applications," *Surface and coatings technology*, vol. 131, pp. 79-83, 2000.

[4] S. H. Bae, C. H. Lee, R. Clark, and D. L. Kwong, "MOS Characteristics of Ultrathin CVD HfAlO Gate Dielectrics," *IEEE Electron Device Letters*, vol. 24, pp. 556~558, 2003.

[5] R. S. Johnson, G. Lucovsky, and I. Baumvol, "Physical and electrical properties of noncrystalline Al2O3 prepared by remote plasma enhanced chemical vapor deposition," *J. Vac. Sci. Technol. A*, vol. 19, pp. 1353-1360, 2001.

[6] H. N. Alshareef, H. F. Luan, K. Choi, H. R. Harris, H. C. Wen, M. A. Quevedo-Lopez, P. Majhi, and B. H. Lee, "Metal gate work function engineering using AlN[sub x] interfacial layers," *Applied Physics Letters*, vol. 88, pp. 112114, 2006.

[7] H.-S. Jung, *VLSI Technology, 2006. Digest of Technical Papers. 2006 Symposium on*, 2006.

[8] K. Lee, M. Frank, V. Paruchuri, E. Cartier, B. Linder, N. Bojarczuk, X. Wang, J. Rubino, M. Steen, P. Kozlowski, J. Newbury, E. Sikorski, P. Flaitz, M. Gribelyuk, P. Jamison, G. Singco, V. Narayanan, S. Zafar, S. Guha, P. Oldiges, R. Jammy, and M. Ieong, "Poly-Si/AlN/HfSiO Stack for Ideal Threshold Voltage and Mobility in Sub-100 nm MOSFETs," presented at VLSI Technology, 2006. Digest of Technical Papers. 2006 Symposium on, 2006.

[9] T. H. Cha, D. G. Park, T. K. Kim, S. A. Jang, I. S. Yeo, J. S. Roh, and J. W. Park, "Work function and thermal stability of Ti1-xAlxNy for dual metal gate electrodes," *Applied Physics Letters*, vol. 81, pp. 4192-4194, 2002.

[10] H. N. Alshareef, K. Choi, H. C. Wen, H. Luan, H. Harris, Y. Senzaki, P. Majhi, B. H. Lee, R. Jammy, S. Aguirre-Tostado, B. E. Gnade, and R. M. Wallace, "Composition dependence of the work function of Ta[sub 1 - x]Al[sub x]N[sub y] metal gates," *Applied Physics Letters*, vol. 88, pp. 072108, 2006.

[11] J. C. Schuster and H. Nowotny, "Phase relationships in the ternary systems (V, Cr, Mo, W, Mn, Re)-Al-N," *Journal of Materials Science*, vol. 20, pp. 2787-2793, 1985.

[12] S. Zafar, C. Cabral, A. R., and A. Callegari, "A method for measuring barrier heights, metal work functions and fixed charge densities in metal/SiO2/Si capacitors," *Applied Physics Letters*, vol. 80, pp. 4858-4860, 2002.
[13] H. C. Wen, R. N. Choi, G. A. Brown, T. Boscke, K. Matthews, H. R. Harris, K. Choi, H. N. Alshareef, H. F. Luan, G. Bersuker, P. Majhi, D. L. Kwong, and B. H. Lee, "Comparison of effective work function extraction methods using capacitance and current measurement techniques," *Ieee Electron Device Letters*, vol. 27, pp. 598-601, 2006.
[14] H. Alshareef, H. Harris, H. Wen, C. Park, C. Huffman, K. Choi, H. Luan, P. Majhi, B. Lee, R. Jammy, D. Lichtenwalner, J. Jur, and A. Kingon, "Thermally Stable N-Metal Gate MOSFETs Using La-Incorporated HfSiO Dielectric," *VLSI Technology, 2006. Digest of Technical Papers. 2006 Symposium on*, pp. 7-8, 2006.
[15] H. Ono, *Applied Physics Letters*, vol. 78, pp. 1832, 2001.
[16] N. Kimizuka, *VLSI Technology, 1999. Digest of Technical Papers*, pp. 73, 1999.
[17] L. Pantisano, T. Schram, B. O'Sullivan, T. Conard, S. D. Gendt, G. Groeseneken, P. Zimmerman, A. Akheyar, M. M. Heyns, S. Shamuilla, V. V. Afanas'ev, and A. Stesmans, "Effective work function modulation by controlled dielectric monolayer deposition," *Applied Physics Letters*, vol. 89, pp. 113505, 2006.
[18] V. Narayanan, V. Paruchuri, N. Bojarczuk, B. Linder, B. Doris, Y. Kim, S. Zafar, J. Stathis, S. Brown, J. Arnold, M. Copel, M. Steen, E. Cartier, A. Callegari, P. Jamison, J.-P. Locquet, D. Lacey, Y. Wang, P. Batson, P. Ronsheim, R. Jammy, and M. Chudzik, "Band-Edge High-Performance High-k/Metal Gate n-MOSFETs Using Cap Layers Containing Group IIA and IIIB Elements with Gate-First Processing for 45 nm and Beyond," *VLSI Technology, 2006. Digest of Technical Papers. 2006 Symposium on*, pp. 178-179, 2006.
[19] Y. Yamamoto, K. Kita, K. Kyuno, and A. Toriumi, "Study of La concentration dependent Vfb shift in metal/HfLaOx/Si capacitors," *International Conference on Solid State Devices and Materials 2006*, pp. 212, 2006.

CHAPTER 6

IMPACT OF METAL GATE ON DEVICE PERFORMANCE AND RELIABILITY

6.1 INTRODUCTION

The use of metal gate in place of poly-Si with high-k dielectrics has been shown to improve overall device performance, and reliability [1]. With the use of metal gate electrodes, improvement in electron mobility is observed possibly due to a reduction in the dielectric defect density or suppression of soft optical phonon scattering [2]. However, studies on comparison of impact on device performance from various metal electrodes has shown to strongly depend on the metal gate [3]. Variations in the metal gate can contribute to changes in the SiO_x interface layer quality, defect trap density in the high-k and roughness at the metal/high-k interface [4, 5]. Since the initial goal of obtaining band edge EWF metal gate were to enable EOT scaling with maximized drive current, it is crucial to study the impact of electrodes on transistor device performance as well as its implications on reliability. The device performance for our proposed n/p-type metal gate candidates had been discussed in Chapter 5. In this chapter, the impact of the EWF engineering species on the reliability of the devices will be discussed. Moreover, studies of other materials systems which would give implications of possible impact of metal gate electrodes on the device reliability is also performed.

6.2 IMPACT OF METAL GATE PROCESSES

The candidate metal gate material systems are mainly PVD metal electrodes. The reliability of any potential band-edge metal gate deposited by PVD may be a concern,

since plasma damage has been an issue for PVD metal electrode films. Park et al.[6] have compared the device performance of atomic layer deposited (ALD) versus PVD WN and TaN. The difference for a higher leakage current and lower G_m observed for PVD metals is attributed to process plasma induced damage. Since Ta and W are metals with large mass which will sputter with higher incident energies and induce greater damage to the dielectric. However, if the PVD processing is fine controlled by a low power deposition process, sputtering damage can be significantly reduced. In this study, the device performance and reliability of a controlled PVD TaN film is compared with TaN deposited by an ALD process.

Experimental procedure

Transistor devices are formed in a standard planar gate-first process scheme. The gate dielectric is ALD HfO_2 and the metal gate is PVD TaN or ALD TaN. All transistor gates are capped with 100nm of polysilicon and endure the full 1000^{o}C poly and S/D activation anneal. PVD deposition of the TaN was performed in a DC sputter tool with a Ta target and Ar/N_2 co-flow. ALD deposition was performed by surface saturation of metal-organic precursor, followed by reduction using ammonia [4].

Results and Discussion

The effective work function of the TaN metal system has been shown to be roughly a mid-gap metal. Figure 6.1 shows the flat band versus EOT plot of 1:1 stoichiometric ALD and PVD TaN deposited on ALD HfO_2 and a similar EWF value is observed. The actual transistor devices show a similar EOT (~1.2 nm for PVD TaN and 1.35nm for ALD TaN) and the threshold voltage (V_t) is similar consistent with the EWF. This is important for determining whether the PVD process induces additional charges in

the dielectric that do not change the flat band voltage but have a deleterious effect on the threshold voltage. The V_t as a function of gate length for the long channel devices is shown in Figure 6.2(a). A tight V_t distribution indicates that the short channel devices are working even with PVD electrode. The accumulation leakage current of large area capacitors (A=5E^{-5} cm^2, same wafer) is shown in Figure 6.2(b). The leakage current of the PVD TaN gate stack (Jg= -2E-1 A/cm^2) is slightly higher than that of the ALD TaN gate stack (Jg= -8E-2 A/cm^2) at V_{fb}-1V. This difference is relatively small, but the PVD electrode sample shows slightly higher current possibly due to the slightly lower EOT. In this case it can be concluded that PVD metal process has minimal effects on the gate stack EOT and V_t as compared to ALD.

The 10μm x 1μm transistor I_d-Vg curves are shown in Figure 6.3(a). The saturation current for the PVD TaN device is significantly higher than the ALD TaN (log scale). This is also reflected in the offset, where across a large sample set the distribution is ~10% higher for the PVD case. Both devices have low sub-threshold swing (SS), 73 mV/dec for the ALD device and 71mV/dec for the PVD device, a strong indicator that he Si interface is very high quality across device structure [7]. This is confirmed by the charge pumping data (1MHz) in Figure 6.3(b), where the PVD device has slightly lower interface states density. However, both devices are in the low 10^{10} eV^{-1} cm^{-2} range, and thus the difference can be considered negligible.

Another metric that can be used to probe the quality of the gate dielectric is a constant voltage stress of transistor devices. We have shown that, during positive constant voltage stress, charge trapping is the dominant mechanism for the threshold voltage instability of high-k devices [4, 10]. Furthermore, this is recoverable with the appropriate negative bias to de-trap electrons from shallow traps. Figure 6.4 depicts the change in threshold voltage at 90^{o}C with +1.8V stress, followed by a relaxation period

with 0V applied. There is a threefold increase in the change in threshold voltage for the ALD TaN. To understand the source of the threshold voltage change, the sub-threshold voltage of the I_d-V_g curves is calculated and shown on the right axis. Since the ΔSS density increase is a good indicator of the amount of interface state density increase, it is apparent from the small change for both cases (<1%) that the source of charges that are increasing threshold voltage is due to trapped charge in the dielectric. From this, it can be concluded that the amount of transient charge trapping is significantly reduced when PVD TaN is used. Furthermore, the dielectric quality is not compromised by the PVD deposition of a heavy metal. This is in contradiction to previous reports, but may be attributed to the high quality of the controlled sputtering process used in this case.

Conclusion

It is shown that, given the right metal PVD deposition conditions, the dielectric is not adversely affected by sputtering of the metal gate when compared to ALD deposition. Highly scaled transistor devices have a low EOT, excellent overdrive current and superior interface properties independent of metal deposition. The PVD TaN transistors display an improved mobility and charge trapping characteristics when compared to ALD TaN transistors and the implementation of PVD, even when sputtering heavy elements, is not precluded based on the quality of transistors and improvement in reliability. And therefore candidate metal gate material systems can be deposited by PVD without roadblocks in the reliability.

6.3 METAL GATE ON BULK HIGH-κ: CHARGE TRAPPING

Electron mobility degradation and V_t instability due to fast transient charging (FTC), which occurs at pre-existing electron traps, are one of the major concerns for implementing high-k dielectrics. The physical origin of these electron traps in the Hf-based high-k stack (ex. HfO_2) is unclear, but has been proposed to be related to dielectric lattice defects such as positively charged oxygen vacancies, as well as the crystallinity of the high-k dielectric [11-13]. Optimization of the HfO_2 processing such as N incorporation [14] or use of $HfSiO_xN_y$ [13, 15] have shown to reduce the charge trapping effects. Interestingly, metal electrodes are found to add additional complexity to this problem due to the interaction between metal electrode and high-k dielectric stacks [16] or changes in the gatestack from the metal electrode process [5]. In this work, a correlation between the source of FTC and physical changes in the gate stack is investigated by studying the impact of metal gate electrodes on mobility degradation. $HfSi_x$ deposited by chemical vapor deposition (CVD) is found to induce oxygen scavenging in the dielectric, and oxygen vacancies formed within the dielectric stack could in turn increase FTC.

Experimental procedure

Gate first N-MOS transistor devices with high channel doping (3E17/cm^3) were fabricated using a standard CMOS process with the 1000^{o}C anneal for dopant activation. 2nm HfO_2 film was deposited by ALD on an ozone pre-treated interface followed by a 700^{o}C N_2 post deposition annealing (PDA). The metal electrodes used in this study are 10nm ALD TiN or 5nm $HfSi_x$ deposited by CVD. Metal electrodes are capped with doped poly-Si for ease of process integration. Transistors with the ALD TiN gate electrodes are used as a control sample in this study due to its excellent stability with

HfO_2 and good device performance [13]. CVD $HfSi_x$ is evaluated as a metal electrode for its application as a n-type electrode low effective work function (4.3eV, ALD TiN work function ~4.5eV). Since the CVD $HfSi_x$ is deposited from a metal organic precursor, it contains certain amount of C and N, but will be noted as $HfSi_x$ for simplicity.

Results and Discussion

Figure 6.5 compares mobility values extracted using the mob2D program [17] from the DC and pulsed I_d-V_g measurements for both the TiN and $HfSi_x$ samples with the universal SiO_2 model. The effective oxide thicknesses (EOT) for both $HfSi_x$ and TiN samples are similar, of 1.07~1.1nm. However, DC mobility of the CVD $HfSi_x$ is clearly degraded compared to the ALD TiN control sample [18]. In the case of high-k dielectrics, sources contributing to DC mobility degradation include a) loss of inversion layer charge due to fast transient charge trapping, b) quality of the interfacial SiO_x and c) phonon scattering, etc. [11, 19]. Inversion charge loss due to FTC has been previously found to be the dominant factor of DC mobility degradation, the charge trapped in the high-k dielectric and screened by the IL from the channel electrons does not influence the intrinsic mobility as had been demonstrated by the ultra short pulse measurements [20]. Previous reports have shown the metal deposition process may change the thickness of the bottom interfacial SiO_x layer, while its thickness is known to strongly affect FTC [21]. However, high-resolution transmission electron microscopy (HRTEM) data of the TiN and $HfSi_x/HfO_2/SiO_x$ stacks show that both samples exhibited similar HfO_2 and bottom SiO_x thicknesses (Figure 6.6(a)(b)), suggesting that variation in physical dimensions is not responsible for the observed difference in mobility of the TiN and $HfSi_x$ samples.

To characterize the FTC influence on mobility characteristics, the I_d-V_g measurements were performed on transistors with W/L=10/1um by the conventional DC method, and using the single pulse I_d-V_g and ultra-short pulse I_d-V_g methods as reported in [20, 22, 23] , to characterize the influence ofcharge trapping on mobility characteristics.

Figure 6.7 shows the drain current I_d as a function of gate voltage and time when a trapezoidal pulse is applied to the gate (V_g). Monitoring the I_d during the flat pulse-width (~100μs) portion of the I_d-time plot, degradation in the I_d (ΔI_d) in the $HfSi_x$ sample is clearly observed. Negligible I_d degradation in the TiN control sample suggests that intrinsically the 2nm HfO_2 does not exhibit charge trapping, and charge trapping in the $HfSi_x$ sample is induced by the CVD $HfSi_x$ electrode. The single pulse technique with fast (5μs) up-and down traces during the V_g sweep, minimizes the effect of FTC/de-trapping and the I_d-V_g dependence obtained during the fast V_g up-trace should be free from FTCE. Therefore, mobility extracted from the single pulse I_d-V_g data shows a mobility improvement compared to the DC I_dV_g measurement for the $HfSi_x$ stack, while no change is observed for the TiN control (Figure 6.5). On the other hand, mobility extracted from the ultra-short pulse (~35ns rise time) measurements show a full recovery to the TiN control, indicating fast trapping may occur on the order of few microseconds or less, and $HfSi_x$ electrode did not influence the "intrinsic" mobility of the stack. In the study of FTCE, the trapped charges have been identified to be located in the bulk portion of the high-k film [24]. Analysis of the nature of these charge traps using the charge trapping model by Bersuker et al. [25] (

Figure 6.7 amplification of ΔI_d), yields a trap capture cross section (σ)~9E-14cm^2, similar to that reported for the TiN electrode sample, suggesting identical nature of traps in the high-k dielectrics for both electrode stacks. However, the bulk high-k trap density

(N_o) in the $HfSi_x$ sample ~2E22/cm^3, is higher than the TiN sample (1E22/cm^3) indicating increased defects induced in the high-k from $HfSi_x$.

For further investigation, the quality of interfacial oxide is compared using the fixed amplitude charge pumping (CP) method at various frequencies (Figure 6.8(b)) [26]. The density of traps at high frequencies, which correspond to the trap location near the interface with the substrate, is similar in the TiN and $HfSi_x$ samples. A gradual increase in N_{it} is observed at lower frequencies towards the HfO_2/SiO_x interface [24, 26, 27]. However, the $HfSi_x$ sample exhibits a slightly higher N_{it} than the TiN control, and previous results indicate interfacial oxides with similar trap density differences only exhibit 5% drive current differences. Therefore, Nit differences cannot completely explain the mobility degradation [26].

CVD $HfSi_x$ process with higher Hf concentration is found to exhibit the "oxygen gettering" or "scavenging" effect from the interfacial SiO_x layer as shown in the HRTEM in Figure 6.6(c). The oxygen gettering effect has been commonly reported due to the high energy of oxide formation and high oxygen solubility of Hf, resulting in the reduction of the gate dielectric and subsequent oxygen diffusion to the gate electrode [28, 29]. Since O diffusion via oxygen lattice exchange is the predominant diffusion mechanism in HfO_2 [30], the O scavenging effects will result in O depletion in both the bulk of HfO_2 and the interfacial SiO_x. In the case of our samples shown in Figure 6.6(b), the oxygen gettering effect is not visible via imaging since the interfacial SiO_x thickness remains similar to the control. However, the higher N_{it} observed in the $HfSi_x$ sample at lower frequencies correlates to an increased degree of interaction, possibly indicating enhanced O scavenging effects in the $HfSi_x$, and its effect is more pronounced closer to the high-k/electrode side. Due to increased charge trapping, reliability degradation is also observed in the PBTI characteristics for samples heavily impacted by

the electrode (Figure 6.9(a)). On the other hand, the FTCE effect is found to be significantly reduced with minimal I_d degradation during the pulsed measurements when oxygen scavenging is suppressed using nitrogen incorporation in high-k film by NH_3 post high-k deposition annealing (Figure 6.9(b)). These results indirectly support our assumption that the $HfSi_x$ electrode generate oxygen vacancies in high-k layer and results in increased FTC behaviors through the oxygen scavenging effect. Elemental diffusion of Hf (from $HfSi_x$) inducing dielectric degradation or N diffusion (from TiN) resulting in improvement of the dielectric quality have also been considered as possible factors. However, Hf from CVD process is believed to be thermal dynamically less mobile, and if diffused should result in increase in the physical thickness of the HfO_2. N incorporation from TiN is found to be a minimal 1-2%, and thus cannot completely explain the electron mobility differences [15].

Conclusion

Physical and electrical analysis of the gate stacks suggests that the significant increase of FTC in $HfSi_x$ may be attributed to higher density of the O vacancies in the high-k dielectric caused by the $HfSi_x$ induced O scavenging process. Through this study, additional influence of metal electrodes on device performance has been identified, and hopefully will provide insight into the choice of candidate metal electrode materials, where material systems with better O stability with the dielectric will be preferred.

6.4 RELIABILITY FOR P-METAL CANDIDATE SYSTEM

One PMOS metal gate scheme is though engineering the metal/dielectric interface. Previously, we show that using aluminum oxide TIL as the engineered interface

drastically reduces threshold voltage (despite an increase in equivalent oxide thickness). Once a viable scheme such as this has been identified, it still must undergo full rigorous reliability screening before it can be properly implemented in any application. We further will look at the impact of this scheme on the negative bias temperature instability (NBTI) and time-dependent dielectric breakdown (TDDB) to evaluate its possibility for 32 nm applications.

Experiment Procedures

Devices were processed in a gate first CMOS flow. After pre-gate clean and an ozone treatment that produces ~1 nm interfacial SiO_2, 2.5 nm of ALD $HfSiO_x$ were deposited. An AlO_X capping layer was then deposited, followed by 20 nm ALD TiN, and then polysilicon. The transistors were subjected to a source/drain spike anneal and forming gas anneal. The reference wafer did not receive the AlO_X layer to compare threshold voltage and EOT.

Results and Discussion

Corresponding transistor C-V curves for the TIL structure and the reference TiN device in Figure 6.10(a) illustrate that, despite the addition of AlO_X, which adds ~2 Å to the EOT, the V_{fb} and V_t of the devices is lowered. Final realization of the V_t benefit of the TIL structure is depicted in Figure 6.10(b), where we see that there is ~200 mV of V_t shift relative to the reference TiN device.

Since this is an option for PMOS stacks, NBTI is one of the foremost concerns. Figure 6.11(a) shows the voltage dependence of constant voltage stress on the V_t at room temperature. After an aggressive stress of -2.05 V, the threshold voltage changes by only ~20 mV. The log-log slopes are parallel across the voltage range shown, with n = 0.15

[31]. In comparing previously reported values [32] for the slope with physical high-k thickness in Figure 6.11(b) , we see that the AlO_x layer in the TIL structure does not change the nature of NBTI for a comparable physical thickness of high-k. Comparing similar stress field, no significant difference in the maximum transconductance degradation is observed with the TIL. This suggests interface degradation is not key contribution to ΔV_t changes. The temperature dependence of NBTI measured for a stress voltage of –2.2 V. The dependence is parallel across temperatures, and the activation energy (Figure 6.12) of $E_a = 0.045$ eV is in agreement with previous results for comparable physical thickness [32]. The low value of E_a suggests that some additional charge trapping is contributing to the V_t stability, which can be a result of the increased physical thickness. It is likely that the ΔV_t occurs because of a combination of charge trapping and interface state degradation. There is a possibility of the introduction of charge centers into the dielectric if Al diffuses. However, this contribution would be very evident in NBTI, and the comparison between similar thicknesses of high k suggests that Al does not contribute to the transistor degradation.

TDDB data in Figure 6.13 show that the breakdown is specific to a single mechanism, as indicated by the vertical distribution of the Weibull plots. Intrinsic defects are expected to dominate the breakdown characteristics. Calculating the 10-year operating voltage at the 63% (zero) crossing point of the Weibull plots, we estimate that this structure can still withstand –1.6 V, well within the V_D+0.2 limit.

Conclusion

The correct implementation of an interface layer at the metal/dielectric interface, in this instance AlO_x, has the net effect of reducing the threshold voltage by >200mV viable for dual metal CMOS applications as a p-type metal. Main reliability concerns

associated with Al-containing stacks are consistent with those observed for comparable thickness of Hf-based high-k. Al is not found to be a roadblock in the PMOS reliability, and should apply to the metal-Al-nitride metal gate systems. Scaling the dielectric to 32 nm specifications with excellent reliability can be realizable.

6.5 FIGURES

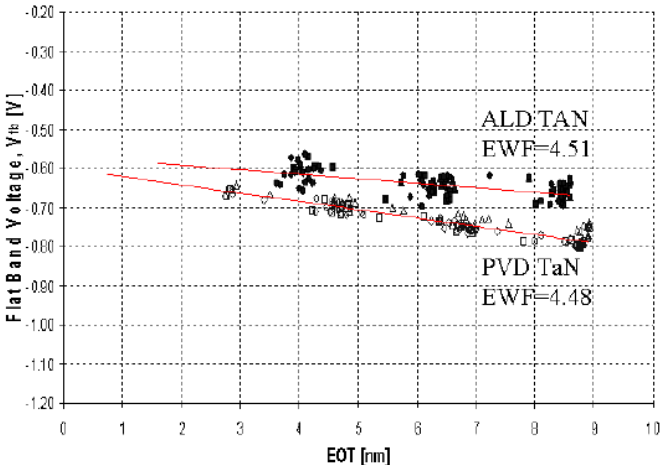


Figure 6.1 Flat band voltage versus EOT for ALD (closed symbols) and PVD (open symbols) TaN on HfO_2.

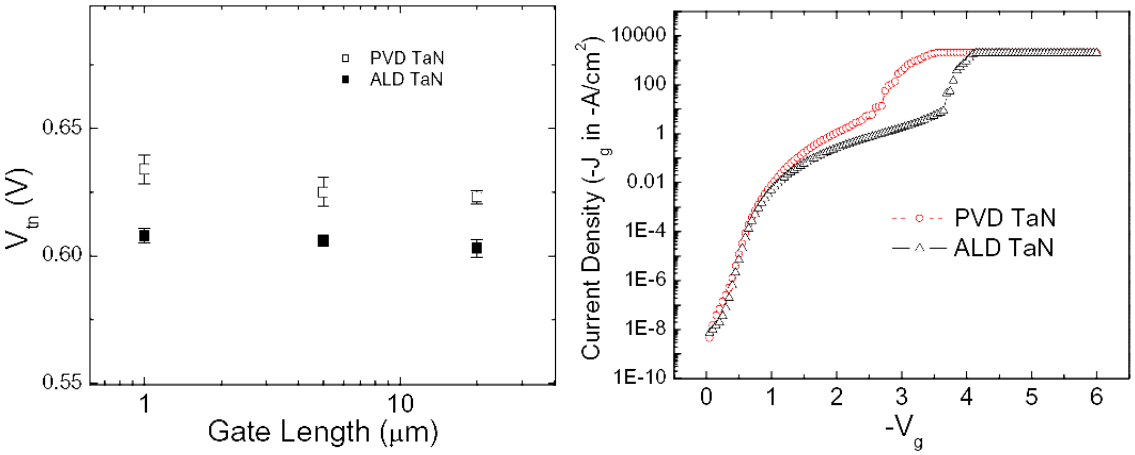


Figure 6.2 Threshold voltage variation for the long channel devices. Accumulation Jg for the ALD and PVD TaN transistors.

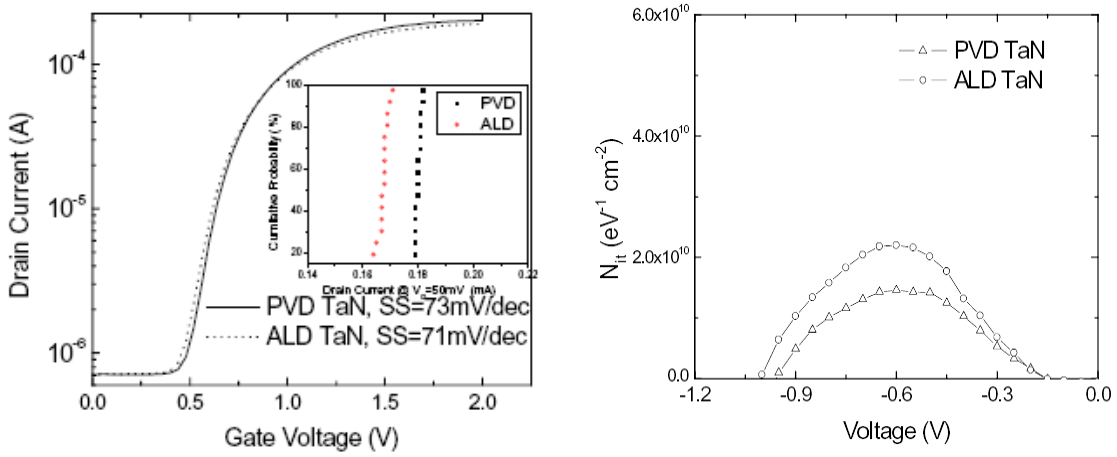


Figure 6.3 (a) I_d-V_g of the two metal gate transistors (b) Charge pumping (1MHz) comparison of the two metal deposition methods.

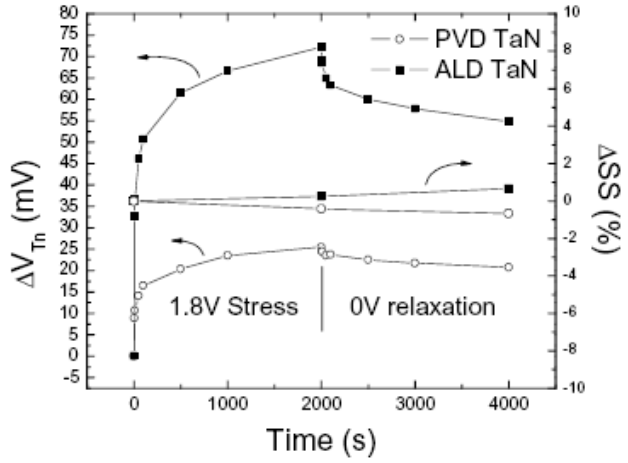


Figure 6.4 Constant voltage comparison at 90°C for the two gate stack device, indicating similar charge trapping characteristics.

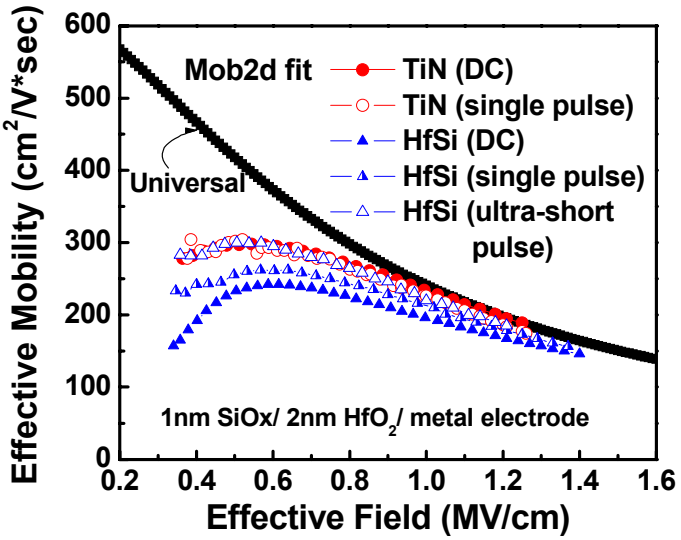


Figure 6.5 Effective mobility plot for $HfSi_x$ electrodes and TiN control modeled by with the DC, single pulse and ultra-short pulse I_d-V_g measurements.

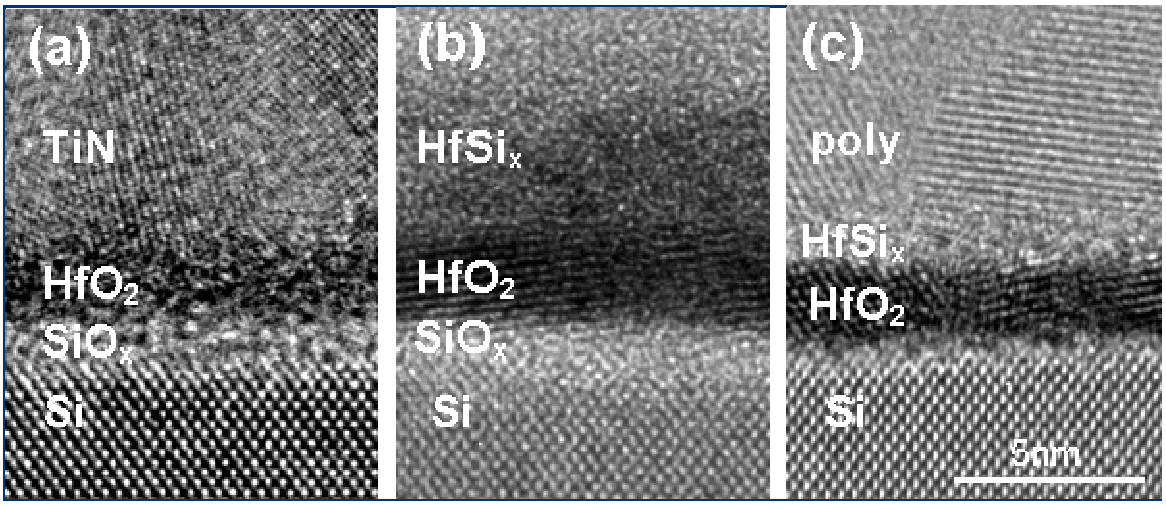


Figure 6.6 HRTEM image of the (a) TiN (b) $HfSi_x$ electrode on 2nm HfO_2. to compare the high-k/ interfacial oxide thicknesses, and (c) CVD $HfSi_x$ with higher Hf content showing reduction in the interfacial oxide thickness from O scavenging effects

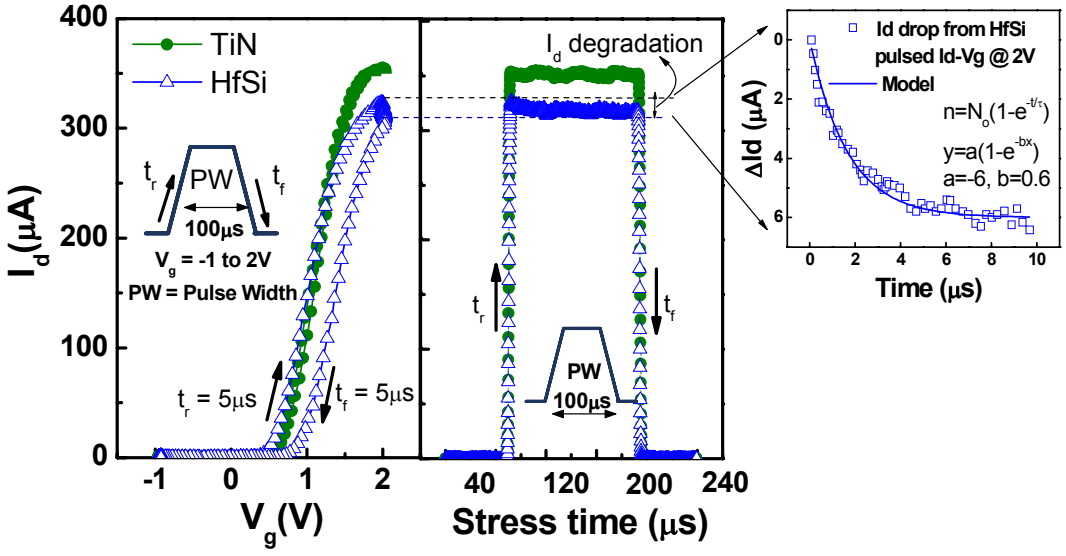


Figure 6.7 Comparison of the single pulse I_d-V_g curve of the TiN and $HfSi_x$ samples. Insert shows schematic of the pulse V_g time dependence, t_r, t_f and PW corresponding to the pulse rise, fall and width times, respectively. Change in I_d during the gate pulse voltage shown on the right for the $HfSi_x$ sample. Model of the I_d current drop during gate pulse performed in blown-up plot.

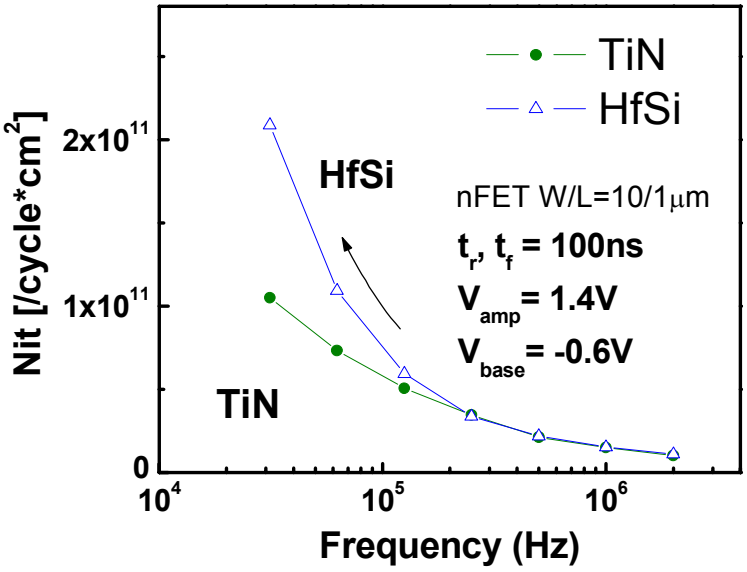
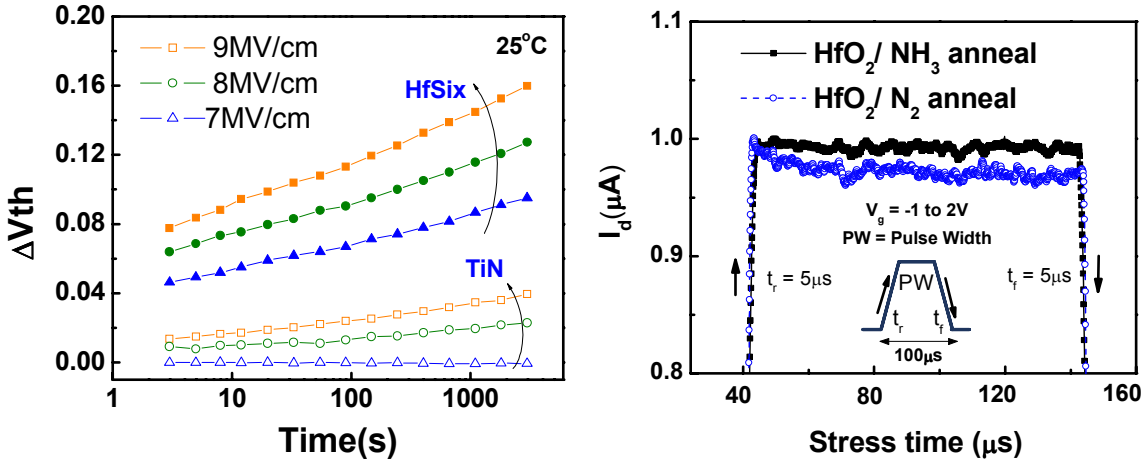
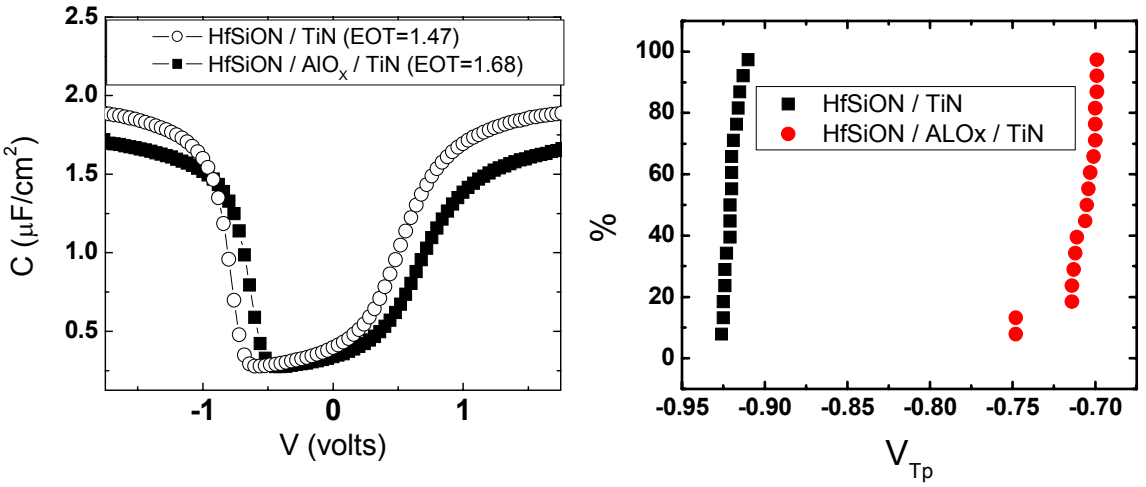


Figure 6.8 Fixed amplitude charge pumping data taken at different frequencies for TiN and $HfSi_x$.



(a) (b)

Figure 6.9 (a) PBTI results for HfSix metal stacks compared to TiN control (b)Single pulse I_d-V_g curve for HfSix gated high-k stacks with (NH_3 post high-k deposition anneal) and without (N_2 anneal) N incorporation.



(a) **(b)**

Figure 6.10 (a) C-V characteristics of the transistors highlight the V_{fb} and V_t shift. (b) The threshold voltage shift is over 200 mV with the AlO_x insertion.

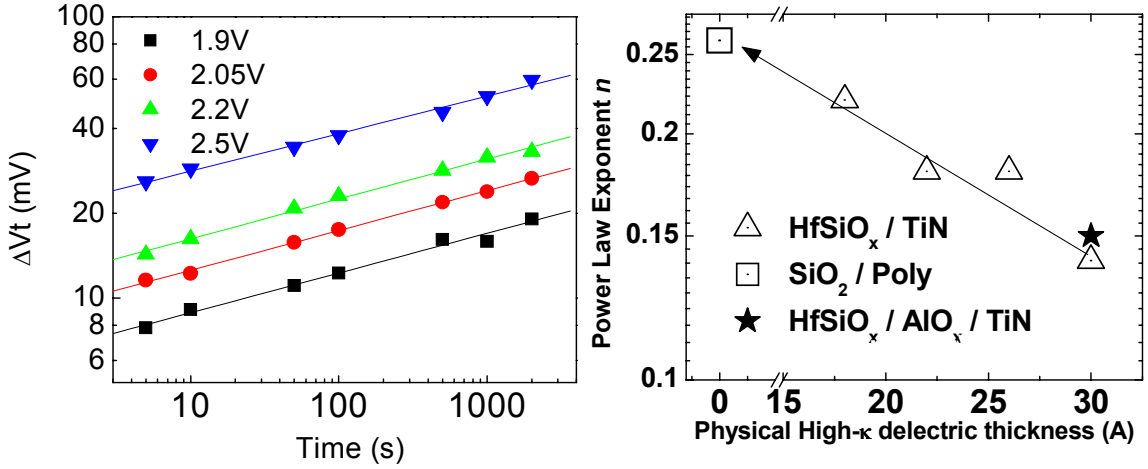


Figure 6.11 **(a) Voltage dependence of CVS is parallel with time, showing a power law dependence. (b) : Power law factor n is comparable to previous data for similar high-k thicknesses**

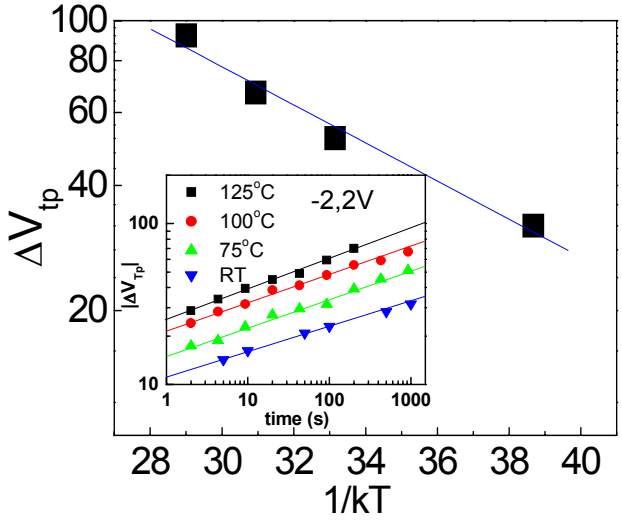


Figure 6.12 **Temperature dependence of NBTI (bias condition) . Activation energy of NBTI indicates charge trapping is occurring, a problem that can be solved with appropriate scaling.**

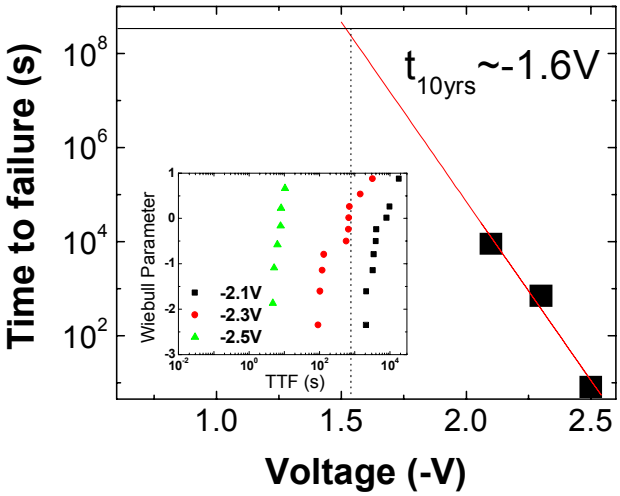


Figure 6.13 TDDB has vertical distribution in the Weibull plots for the TIL structure. A respectable 10-year operating voltage of –1.6 V is extracted from TDDB.

6.6 REFERENCES

[1] R. Chau, S. Datta, M. Doczy, B. Doyle, J. Kavalieros, and M. Metz, "High-kappa/metal-gate stack and its MOSFET characteristics," *Ieee Electron Device Letters*, vol. 25, pp. 408-410, 2004.

[2] R. Chau, S. Datta, M. Doczy, B. Doyle, J. Kavalieros, and M. Metz, "High-k/Metal–Gate Stack and Its MOSFET Characteristics," *IEEE Electron Device Letter*, vol. 25, pp. 408-410, 2004.

[3] A. C. V. Narayanan, F.R. McFeely, K. Nakamura, P. Jamison, S. Zafar, E. Cartier, A. Steegen, V. Ku, P. Nguyen, K. Milkove, C. Cabral Jr., M. Gribelyuk, C. Wajda, Y. Kawano, D. Lacey, Y. Li, E. Sikorski, E. Duch, H. Ng, C. Wann, R. Jammy, M. Ieong, G. Shahidi, "Dual Work Function Metal Gate CMOS using CVD metal electrodes," *VLSI Technology Digest*, pp. 192-193, 2004.

[4] C. Young, G. Bersuker, H. C. Wen, G. Brown, and P. Majhi, "Charge Trapping Characteristics of Hafnium Based High-ê Dielectrics with Various Metal Electrodes," *SSDM 2004*, 2004.

[5] P. Majhi, C. Young, G. Bersuker, H. C. Wen, G. A. Brown, B. Foran, R. Choi, P. M. Zeitzoff, and H. R. Huff, "Influence of Metal Gate Materials and Processing on Planar CMOS Device Characteristics with High-k Gate Dielectrics," *ESSDERC*, 2004.

[6] D.-G. Park, Z. J. Luo, N. Edleman, W. Zhu, P. Nguyen, K. Wong, C. Cabral, P. Jamison, B. H. Lee, A. Chou, M. Chudzik, J. Bruley, O. Gluschenkov, P. Ronsheim, A. Chakravarti, R. Mitchell, V. Ku, H. Kim, E. Duch, P. Kozlowski, C. D'Emic, V. Narayanan, A. Steegen, R. Wise, R. Jammy, R. Rengarajan, H. Ng, A. Sekiguchi, and C. H. Wann, "Thermally robust dual-work function ALD-MNx MOSFETs using conventional CMOS process flow," *VLSI Technology Digest*, 2004.

[7] S. M. Sze, *Physics of Semiconductor Devices*: John Wiley & Sons Inc., 1981.

[8] Y. Ma, L. Liu, and Z. Li, "A discussion on the universality of inversion layer mobility in MOSFET's," *Electron Devices, IEEE Transactions on*, vol. 46, pp. 1920-1922, 1999.

[9] P. D. Kirsch, M. A. Quevedo-Lopez, S. A. Krishnan, C. Krug, H. AlShareef, C. S. Park, R. Harris, N. Moumen, A. Neugroschel, G. Bersuker, B. H. Lee, J. G. Wang, G. Pant, B. E. Gnade, M. J. Kim, R. M. Wallace, J. S. Jur, D. J. Lichtenwalner, A. I. Kingon, and R. Jammy, "Band Edge n-MOSFETs with High-k/Metal Gate Stacks Scaled to EOT=0.9nm with Excellent Carrier Mobility and High Temperature Stability," *Electron Devices Meeting, 2006*, pp. s23p4, 2006.

[10] W. Zhu, J.-P. Han, and T. P. Ma, "Mobility measurement and degradation mechanisms of MOSFETs made with ultrathin high-k dielectrics," *Electron Devices, IEEE Transactions on*, vol. 51, pp. 98-105, 2004.

[11] G. Bersuker, J. H. Sim, C. D. Young, R. Choi, B. H. Lee, P. Lysaght, G. Brown, P. Zeitzoff, M. Gardner, R. W. Murto, and H. R. Huff, "Effect of structural properties of Hf-based gate stack on transistor performance," *Materials Research Society Symposium*, vol. 811, pp. 31, 2004.

[12] J. L. Gavartin, A. L. Shluger, A. S. Foster, and G. Bersuker, "The role of nitrogen-related defects in high-k dielectric oxides: Density-functional studies," *Journal of Applied Physics*, vol. 97, pp. 053704-1~12, 2005.

[13] P. D. Kirsch, J. H. Sim, S. C. Song, S. Krishnan, J. Peterson, H. J. Li, M. Quevedo-Lopez, C. D. Young, R. Choi, N. Moumen, P. Majhi, Q. Wang, J. G. Ekerdt, G. Bersuker, and B. H. Lee, "Mobility enhancement of high-k gate stacks through reduced transient charging," *Solid-State Device Research Conference, 2005. ESSDERC 2005. Proceedings of 35th European*, pp. 367-370, 2005.

[14] M. Koike, T. Ino, Y. Kamimuta, M. Koyama, Y. Kamata, M. Suzuki, Y. Mitani, A. Nishiyama, and Y. Tsunashima, "Effect of Hf-N bond on properties of thermally stable amorphous HfSiON and applicability of this material to sub-50nm technology node LSIs," *Electron Devices Meeting, 2003. IEDM '03 Technical Digest. IEEE International*, pp. 4.7.1-4.7.4, 2003.

[15] M. A. Quevedo-Lopez, S. A. Krishnan, P. D. Kirsch, H. J. Li, J. H. Sim, C. Huffman, J. J. Peterson, B. H. Lee, G. Pant, B. E. Gnade, M. J. Kim, R. M. Wallace, D. Guo, H. Bu, and T. P. Ma, "High Performance Gate First HfSiON Dielectric Satisfying 45nm Node Requirements," *IEEE Electron Device Meeting*, vol. 17.4, 2005.

[16] Y. Akasaka, K. Miyagawa, T. Sasaki, K. Shiraishi, S. Kamiyama, O. Ogawa, F. Ootsuka, and Y. Nara, "Impact of electrode-side chemical structures on electron mobility in metal/HfO/sub 2/ MISFETs with sub-1nm EOT," *VLSI Technology, 2005. Digest of Technical Papers. 2005 Symposium on*, pp. 228-229, 2005.

[17] J. R. Hauser, "Extraction of experimental mobility data for MOS devices," *Electron Devices, IEEE Transactions on*, vol. 43, pp. 1981-1988, 1996.

[18] G. Bersuker, P. Zeitzoff, J. H. Sim, B. H. Lee, R. Choi, G. Brown, and C. D. Young, "Mobility Evaluation in Transistors with Charge Trapping Gate Dielectrics," *Applied Physics Letters*, vol. 87, pp. 042905, 2005.

[19] T. Yamaguchi, R. Iijima, T. Ino, A. Nishiyama, H. Satake, and N. Fukushima, "Additional scattering effects for mobility degradation in Hf-silicate gate MISFETs," *IEEE Electron Device Meeting*, vol. Technology Digest, pp. 621-624, 2002.

[20] C. D. Young, R. Choi, J. H. Sim, B. H. Lee, P. Zeitzoff, Y. Zhao, K. Matthews, G. A. Brown, and G. Bersuker, "Interfacial layer dependence of HFSI/sub x/O/sub y/ gate stacks on V/sub T/ instability and charge trapping using ultra-short pulse in characterization," *Reliability Physics Symposium, 2005. Proceedings. 43rd Annual. 2005 IEEE International*, pp. 75-79, 2005.

[21] P. Majhi, H. C. Wen, H. Alshareef, K. Choi, R. Harris, P. Lysaght, H. Luan, Y. Senzaki, S. C. Song, B. H. Lee, and C. Ramiller, "Evaluation and integration of metal gate electrodes for future generation dual metal CMOS," *Integrated Circuit Design and Technology, 2005. ICICDT 2005. 2005 International Conference on*, pp. 69-72, 2005.

[22] C. D. Young, P. Zeitzoff, G. A. Brown, G. Bersuker, B. H. Lee, and J. R. Hauser, "Intrinsic mobility evaluation of high-/spl kappa/ gate dielectric transistors using pulsed I/sub d/-V/sub g/," *Electron Device Letters, IEEE*, vol. 26, pp. 586-589, 2005.

[23] A. Kerber, E. Cartier, L. A. Ragnarsson, M. Rosmeulen, L. Pantisano, R. Degraeve, Y. Kim, and G. Groesenenken, "Direct measurment of the inversion charge in MOSFETs: Application to mobility extraction in alternative gate dielectrics," *VLSI Symosium Tech. Dig.*, pp. 159-160, 2003.

[24] C. D. Young, S. Nadkarni, D. Heh, H. R. Harris, R. Choi, J. Peterson, J. H. Sim, S. Krishnan, J. Barnett, E. Vogel, B. H. Lee, P. Zeitzoff, G. Brown, and G. Bersuker, "Detection of electron trap generation due to constant voltage stress on high-k gate stacks," *International reliability physics symposium*, vol. 3.A.1, 2006.

[25] G. Bersuker, B. H. Lee, H. R. Huff, J. Gavartin, and A. Shluger, "Mechanism of charge trapping reduction in scaled high-k gate stacks," presented at Proceedings of the NATO Advanced Research Workshop on Defects in Advanced High-k Dielectric Nano-Electronic Semiconductor Devices, St. Petersburg, Russia, 2006.

[26] C. D. Young, G. Bersuker, Y. Zhao, J. Peterson, J. Barnett, G. Brown, J. H. Sim, R. Choi, B. H. Lee, and P. Zeitzoff, "Probing stress effects in HfO2 gate stacks with time dependent measurements," *Microelectronics Reliability*, vol. 45, pp. 806-810, 2005.

[27] R. Degraeve, A. Kerber, E. Cartier, L. Pantisano, and G. Groesenenken, "Effect of bulk trap density on HfO2 reliability and yield," *IEEE Electron Device Meeting*, pp. 935-938, 2003.

[28] V. Misra, G. P. Heuss, and Z. H., "Use of metal-oxide-semiconductor capacitors to detect interactions of Hf and Zr gate electrodes with SiO2 and ZrO2," *Applied Physics Letters*, vol. 78, pp. 4166-4168, 2001.

[29] C. Choi, C. Y. Kang, S. J. Rhee, M. Akbar, S. Krishnan, M. Zhang, H. Kim, T. Lee, I. Ok, F. Zhu, and J. C. Lee, "Aggressively scaled ultra thin undoped HfO2 gate dielectric (EOT<0.7nm) with TaN gate electrode using engineered interface layer," *IEEE Electron Device Letters*, vol. 26, pp. 454-456, 2005.

[30] L. V. Goncharova, M. Dalponte, D. G. Starodub, T. Gustafsson, E. Garfunkel, P. S. Lysaght, B. F. Barnett, and G. I. Bersuker, "Oxygen diffusion and reactions in Hf-based dielectrics," *Applied Physics Letters*, vol. 89, pp. 044108, 2006.

[31] J. H. Sim, S. C. Song, P. D. kirsch, C. D. Young, R. Choi, D. L. Kwong, B. H. Lee, and G. Bersuker, "Effects of ALD HfO2 thickness on charge trapping and mobility," *Insulating films on semiconductors INFOS 2005*, pp. 8.1, 2005.

[32] S. A. Krishnan, M. Quevedo, R. Harris, P. D. Kirsch, R. Choi, B. H. Lee, G. Bersuker, J. Peterson, H.-J. Li, C. D. Young, and J. C. Lee, "NBTI Dependence on Dielectric Thickness in Ultra-scaled HfSiO Dielectric/ ALD-TiN Gate Stacks," *2005 International conference on SOLID STATE DEVICES AND MATERIALS*, pp. A.2-4, 2005.

CHAPTER 7

CONCLUSIONS AND FUTURE WORK

7.1 SUMMARY AND CONCLUSION

Metal gate electrodes have the advantage of eliminating poly depletion and poly/high-k interaction, as well as addressing the issue of high V_t values in pFETs caused by Fermi-level pinning between the poly and high-k. To reduce V_t for maximized drive current, the metal work function values should be near the band-edge of Si, i.e. EWF of ~5.0-5.2eV for p-MOS, and 4.1-4.3eV for n-MOS. A systematic study on the metal gate EWF has been performed with the goal of identifying band-edge metal gate electrode candidates.

Potential error sources in the EWF extraction from high-k thickness series have presented a need for alternative EWF extraction techniques on high-k dielectrics. The terraced oxide technique has been developed and demonstrated as an accurate technique for EWF extraction on high-k. In combination with the leakage current barrier height extraction technique, we are able to distinguish true EWF changes and the impact from gate stack charges. With the terraced oxide technique as the metric for EWF measurement, a study of factors controlling EWF is performed.

Fermi-level pinning is proposed to limit the EWF tuning on high-k dielectrics, and a intrinsic roadblock to the identification of band-edge metal gates on high-k. A summary of literature proposed models of Fermi-level pinning is discussed and compared with our experimental data. It is concluded that an intrinsic limitation (MIGS pinning) should not exist and the source for most EWF pinning on high-k is due to extrinsic contributions, such as interfacial reactions, or possible O vacancy formation induced in

the dielectric. Therefore, through careful control of extrinsic factors, potential band-edge metal gate electrodes could be achieved.

To investigate possible controlling factors on the EWF, analysis based on the systematic breakdown of the EWF equation is performed. EWF is found to not only be controlled by the bulk metal characteristic, but the interface properties between the metal and dielectric exhibits a greater impact on EWF. Charges can be induced in the gate stack during device processing, in addition to intrinsic dielectric charges and shift the V_{fb}. EWF engineering by interface engineering, possibly from formation of an internal dielectric interface dipole, is also identified as a plausible approach for EWF tuning.

Al-containing electrode stacks, either via interface engineering with a AlO_x interface layer between the metal and high-k or in bulk metal-aluminum-nitride form is identified as potential p-type metal gate electrode candidates (EWF=4.95~5.1eV). Lanthanide metal electrode stacks are identified as a suitable n-type metal gate solution (EWF=4.1eV) without compromising device performance.

Comparison of metal gates on device performance and reliability studies are performed. Potential impact of candidate metal gates systems is studied, as well as other material systems which may give implications on the influence of metal gates on the gate stack. Comparison of the deposition technique, shows that even PVD metal electrodes can exhibit high performance. Metal systems which will impact the bulk high-k are materials with high O solubility or reactivity with O. Reduction of the high-k will result in increased charge trapping behavior and degraded electron mobility.

7.2 FUTURE WORK: THE V_{FB} ROLLOFF ISSUE FOR P-TYPE EWF METALS

Although band edge metal electrodes candidates have been identified, a new challenge in the integration for p-type EWF metals is found in the device integration at

low EOT regimes. A gradual reduction in the V_{fb} as the gate stacks are scaled to lower EOT, with the onset of "roll-off" occurring at EOT of ~2-3nm (Figure 7.1(a)). The magnitude of roll-off (ΔV_{fb}) is found to be enhanced with higher EWF (p-type) metals. Compensating for EOT differences from the high-k, the onset of roll-off occurs at similar thicknesses in the interfacial SiO_2. Enhanced roll-off is also observed with increased thermal budget of the gate stacks, pointing to its thermally activated mechanism (Figure 7.1(b)). Interestingly, a similar observation was independently reported by Schaeffer et al. [1], showing an independent confirmation of this phenomenon. Physical mechanisms of this effect may be simply extrinsic (localized material interdiffusion [metal, N, O]), inducing changes in the physical barrier height, or they may be intrinsic and related to communication between the electrode with charge states in the dielectric (generated by O vacancy formation) or induced as the SiO_2 becomes less stoichiometric. The roll-off effect in transistors prevents V_t scaling as EOT reduces (Figure 7.2), and therefore, may require trade-offs in the optimization of p-MOS devices. Resolving the V_{fb} roll-off issue is the key factor to implementing p-MOS metal gate electrodes with a low V_t, and more understanding on the actual mechanism would be required.

7.3 FIGURES

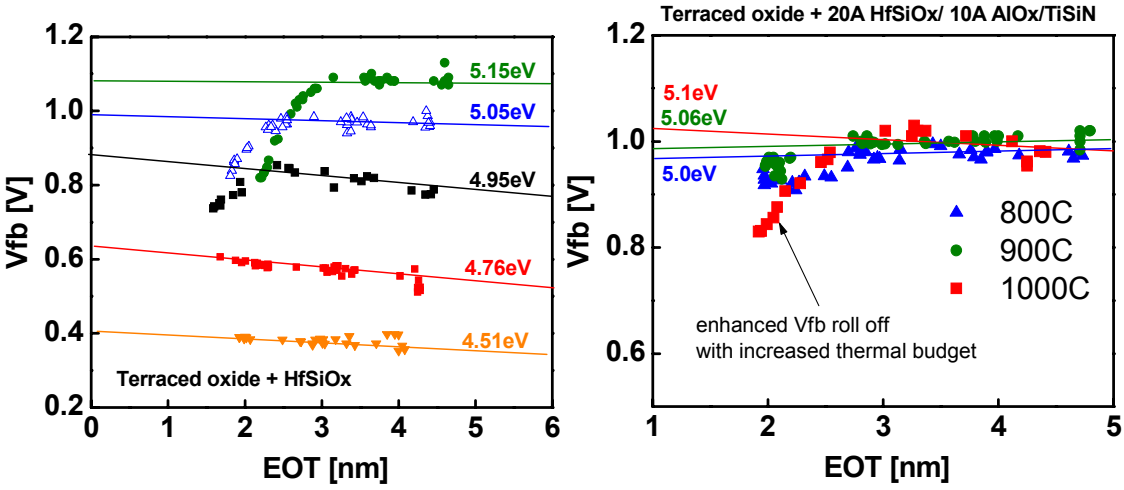


Figure 7.1 (a) V_{fb}-EOT plot for high and low EWF metals showing gradual V_{fb} reduction for high EWF metals. (b) V_{fb}-rolloff as a function of processing temperature

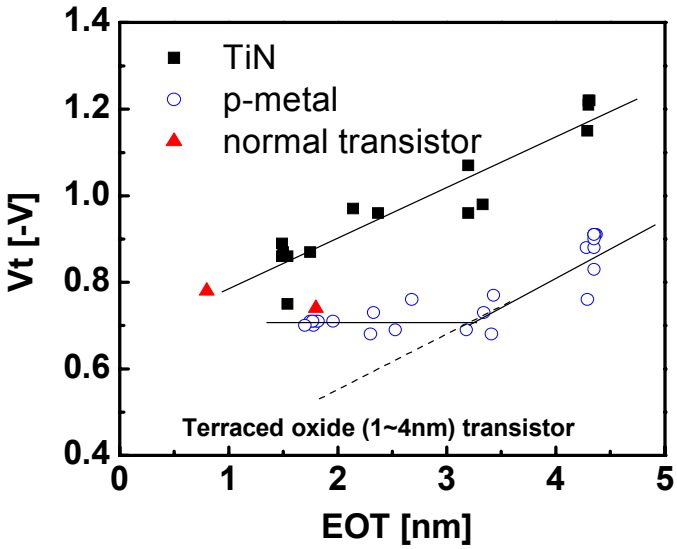


Figure 7.2 V_t-EOT relationship for high/low EWF metals. Rolloff effect is reflected in pMOS V_t values in the low EOT range.

7.4 REFERENCE

[1] J. Schaeffer, D. Gilmer, S. Samavedam, D. Triyoso, R. Hegde, S. Kalpat, M. Raymond, C. Capasso, B. Taylor, M. Sadd, H. H. Tseng, M. Stoker, A. Haggag, D. Roan, L. L. Happ, C. , P. J. Tobin, and B. E. White, "Materials Challenges for High Permittivity Gate Dielectrics and Metal Gate Electrodes," *IEEE ISAGST 2006*, 2006.

Appendix I

	Dielectric / Metal (bulk WF)	SiO2	HfO2	HfSixOy	Si3N4	ZrO2	Al2O3	Ta2O5	other
N-type (<4.6eV)									
Midgap (4.6-4.8eV)	IrO2		5.1-4.76 FG-900C c						
P-type (>4.8eV)	RuO2	5.04 600C fb 5.06 FG c					5.17/5.0 SiO2/Y2O3 FG c		

	Dielectric / Metal (bulk WF)	SiO2
N-type (<4.6eV)	HfSi	4.23-4.87 900C c
	NiSi	undoped: 4.4-4.9 ntype: 4.6 c ptype: 5.1 c undoped: 4.35 800C c
	NbSi2	4.35~4.53
	TiSi	4.3 800C c 4.3
	WSi	4.2~4.65 600C c
	WSi2	4.55~4.8
	TaSi1+x	4.15/4.45 FG/700C
Midgap (4.6-4.8eV)	CoSi2	4.6 vt shift
	MoSi2	4.6 Vt 4.6~4.8, 4.9
	NiSi	undoped: 4.4-4.9 ntype: 4.6 c ptype: 5.1 c undoped: 4.35 800C c
	WSi2	4.55~4.8
P-type (>4.8eV)	HfSi	4.23-4.87 900C c 4.23-4.87 950C c
	NiSi	undoped: 4.4-4.9 ntype: 4.6 c ptype: 5.1 c undoped: 4.35 800C c
	MoSi2	4.6 Vt 4.6~4.8, 4.9
	PtSi	4.9 c 5.1 c

Summary of literature reported EWF values: categorized into 1) Metal Oxides 2) Metal Silicides 3) Pure metals and alloys 4) Metal nitrides

Notations for methods of EWF extraction:

c: capacitor
ip: internal photoemission
fb: estimated by V_{fb} value
Vt (tr): estimated by V_t value
fn: FN tunneling
s: QM simulator for EWF

(FG: measured after forming gas anneal)

	Dielectric → / Metal ↓ (bulk WF)	SiO2	HfO2	HfSixOy	Si3N4	ZrO2	Al2O3	Ta2O5	other
N-type (<4.5eV)	Al 4.28	4.14 c 4.1			4.06 c	4.25 ip			
	Hf 3.95 p	4.0 c							
	Mg 3.66 p	3.45 ip				4.15 ip	3.6 ip		
	Nb 4.3	4.3, 4.0~4.3							
	Ni-Ti (5.4-4.33)	Ni-Ti 5.3 400C c Ti 3.9 400C c							
	Ru-Ta (4.71-4.25)	4.3-5.2 1000C c							
	Ru50Ta50	4.2 800C c 5.2 Ru50Ta50/Ru 800C c							
	Ta 4.25 t	4.2 c 4.35 400C c 4.44 700C						4.25 c 4.33 400C c 4.72 800C c	
	Ti 4.33	3.9 FG c 4.33,4.6 c			4.56 1050C tr			4.17 c 3.91 400C c	
	TiTa	4.16/4.15 400/600C c							
	Zr 4.05	4.05							
Midgap (4.6-4.8eV)	Ir 5.27	4.9 900C c	4.5-4.64 FG-900C c						
	W 4.63 f	4.75 4.55~4.63	4.6-4.7FN 4.7 NMOS pFET Vt -0.5					4.75 c 4.74 400C c 4.77 800C c	
P-type (>4.9eV)	Au 5.31-5.47 p					5.05 ip	5.1 ip		
	Ir 5.27	4.9 900C c	4.5-4.64 FG-900C c						
	Mo 4.95 p	5.05 c	4.95 c	4.77	4.76 c 4.72 1050C tr	4.94		4.64 c 4.78 400C c 4.94 800C c	4.79 (ZrSiO4)
	Ni 5.04 p	5.3 FG c				4.75 ip	4.5 ip		
	NiCu 4.5-5.15 f [27]								
	Ni-Ti (5.4-4.33)	Ni-Ti 5.3 400C c Ti 3.9 400C c							
	Pt 5.65 p	5.59 c 5.2 400C c	5.23 c			5.05 c			
	PtTa (5.65/4.25)	5.05/4.8 400/600C c							
	Re 4.96		PFET Vt -0.4,-0.5						
	RhPt 4.5-5.2 f [27]								
	Ru 4.71	5.3 FG c 5.05 1000C c 4.55 as-dep 4.84	Y 900C c 4.5-5.0		4.5 -5.2		4.98 FG c		
	Ru-Ta (4.71-4.25)	4.3-5.2 1000C c	Y 900C c						

	Dielectric → / Metal ↓ (bulk WF)	SiO2	HfO2	HfSixO	Si3N4	ZrO2	Al2O3	Ta2O5	other dielectrics
N-type (<4.6eV)	TaSiN	4.25 1000C c 4.43 900C c 4.52 600C 4.8 1000C c	4.55 900C c 4.36 1025C 4.4 1000C c				4.84 900C c_tox		
	TaN	4.4-4.7 FG-1000C 3.9 600C 4.5-4.7 950C c 4.0-4.75 950C c 4.2 4.7 1000C	4.34-4.4 FG-1000C c 4.4 1025C c 4.2-4.75 950C c 4.3 4.41 1000C	4.4		4.3 4.5		5.41 c 4.55 400C c	
	TaPN	4.35 600C							
	TiAlN	5.0-5.2 950C c n-4.36 1000C c p-5.13 1000C c							
	TiSiN	4.37 600C							
Midgap (4.6-4.8eV)	HfN	4.71 1000C c	4.8 1000C c						
	MoN	4.94/4.95 NMOS 800C s 4.70/4.53 PMOS 800C s 4.4-5 700+900C c 4.4-4.7 900C c						5.33 c 4.89 400C c 4.7 800C c	
	TaSiN	4.25 1000C c 4.43 900C c 4.52 600C 4.8 1000C c 4.8 (Si>Ta) 900C 4.4 (Ta>Si) 900C	4.55 900C c 4.4 1025C c 4.4 1000C c 4.2				4.84 900C c_tox		
	TaN	4.4-4.7 FG-1000C c 3.9 600C 4.5-4.7 950C c 4.0-4.75 950C c	4.34-4.4 FG-1000C c 4.4 1025C c 4.2-4.75 950C c					5.41 c 4.55 400C c	
	TiN	4.58 900C c 4.48 600C	4.6-4.7 900C c_tox 4.78 c				4.8-4.9 900C c_tox	4.95 c 4.80 400C c 4.81 800C c	
	ZrN	4.6							
P-type (>4.8eV)	MoN	4.94/4.95 NMOS 800C s 4.70/4.53 PMOS 800C s 4.4-5 700+900C c 4.4-4.7 900C c						5.33 c 4.89 400C c 4.7 800C c	
	TaCN	4.94 600C							
	TiAlN	5.0-5.2 950C c n-4.36 1000C c p-5.13 1000C c							
	WN	5.0 5.1 1000C c	4.2-4.35 as-900C c					4.75 c 4.74 400C c 4.77 800C c	

Appendix II

Material properties of metal gate electrodes. 1) n-type WF, 2) p-type WF and 3) Midgap WF

Element	WF(exp)	Melting Point (°C)	Resistivity (ohm-cm)	Compounds (dep/etch-ability)	Capture Cross Section (cm^2)	Trap Energy Levels (eV) hole: above Ev electron: below Ec	Expansion Coefficient ($x10^{-6}k^{-1}$)	Electronic Specific Heat ($mJ\ mol^{-1}k^{-2}$)	Diffusion Coefficient (cm/sec) /Activation energy (eV)	Diffusivity @ 1000°C in Si (cm^2/sec)
~~Te~~	~~4.95~~	~~449~~	~~1000~~				-	-	0.5 / 3.34	< 1e-11
Re	**4.96**	**3186**	**18**	**ReF6(18.5)**	n = 8.5e-16;p = 1.3e-16	a: Ec-0.5/0.3/0.17;Ev+0.18/0.4	6.2	2.3		
Be	**4.98**	**1287**	**4**	**Be3N2(2200)**	p = 4.2e-15	p: 0.43	11.3	0.17		1.00E-07
Rh	**4.98**	**1964**	**4.3**	**RhF6(70)**	n = 8.6e-13	n: Ec-0.353	8.2	4.9		1E-4~1E-6
Co	**5**	**1495**	**6**		n = 6.3e-14	p: Ev+0.22/ 0.29/ 0.4/ 0.45 n:Ec-0.36/ 0.44	13	4.73	9.2e4 / 2.8	7.40E-07
Au	**5.1**	**1064**	**2.2**	**AuF6(60)**	n = 9e-17;p = 1.1e-14	p:Ev+0.33 n:Ec+0.54	14.2	0.729	2.4e-4/ 0.39 2.75e-3/ 2.05	7.5E-6 (inter) 1.9E-11 (sub)
Pd	**5.12**	**1554**	**10**	**PdBr2(250)**	n ~ 1e-14/1e-15	d:Ev+0.33 a:Ec-0.22	11.8	9.42	2.95e-4 / 0.22	1.90E-11
Ni	**5.15**	**1455**	**7**		p = 6.7e-14	a: Ec-0.37; Ev+0.24	13.4	7.02	0.1 / 1.9	1.20E-10
~~As~~	~~5.2~~	~~817~~	~~30~~	~~AsF3(-6)~~	Cn+=8e-6 (4.2k)	n: 0.049	-	0.19	22.9 / 4.1	
Ir	**5.27**	**2466**	**4.7**	**IrF3(250); IrF6(44)**	n = 1.3e-10	n:Ec-0.385	6.4	3.1	0.04 / 1.3	2.86E-07
Pt	**5.65**	**1768**	**10.6**	**PtF6(61)**	n = 3e-14	n: Ec-0.23	8.8	6.8	1.5e2 / 2.2	2.90E-07
~~Se~~	~~5.9~~	~~221~~	~~1000~~		n > 1e-14	n: Ec-0.52			0.95 / 2.6	4.70E-11

Element	WF(exp)	Melting Point (°C)	Resistivity (ohm-cm)	Compounds (dep/etch-ability)	Capture Cross Section (cm^2)	Trap Energy Levels (eV) hole: above Ev electron: below Ec	Expansion Coefficient ($x10^{-6}k^{-1}$)	Electronic Specific Heat ($mJ\ mol^{-1}k^{-2}$)	Diffusion Coefficient (cm/sec) /Activation energy (eV)	Diffusivity @ 1000°C in Si (cm^2/sec)
Cr	**4.5**	**1907**	**12.7**	**Cr2Te3(1300C)**	n = 2.6e-16; p = 3.5e-16	Ec-0.23/Ec-0.24/ Ev+0.11	4.9	1.4	0.01 / 1.0	1.09E-06
Fe	**4.5**	**1538**	**9.7**		n = 1.1e-14;p = 3e-16	p:Ec-0.27 n:Ev+0.4	11.8	4.98	0.0062 / 0.87	2.20E-06
~~Sb~~	~~4.55~~	~~630~~			Cno^+=1.6~2.6e-6	d: Ec-0.039	11	0.11	0.214 / 3.65	
W	**4.55**	**3422**	**5**		n = 1e-16	n: Ec-0.22	4.5	1.3	-	~1e-12
Mo	**4.6**	**2693**	**5**	**MoSe2(>1200); MoN(1750)**	p = 9.3e-16	d: Ev+0.30	4.8	2	-	~2e-10
Cu	**4.65**	**1084**	**1.7**	**Cu2Se(1113)**	p = 3.5e-20	a: Ev+0.24/0.37/0.52	16.5	0.695	0.04 / 1.0	
Tc	**4.7**	**2157**	**20**				-	-		
Ru	**4.71**	**2334**	**7.1**	**RuO2(1200 sublimes); RuO4(25); RuF6(54C)**	n = 1.2e-15;p = 4.4e-15	a:Ec-0.24 d:Ec-0.45	6.4	3.3	-	5.00E-07
Os	**4.83**	**3033**	**8.1**	**OsF6(33)**		a:Ec-0.18 d:Ev+0.18	5.1	2.4	-	2.00E-06

Element	WF(exp)	Melting Point (°C)	Resistivity (8ohm-cm)	Compounds (dep/etch-ability)	Capture Cross Section (cm^2)	Trap Energy Levels (eV) hole: above Ev electron: below Ec	Expansion Coefficient ($x10^{-6}k^{-1}$)	Electronic Specific Heat ($mJ\ mol^{-1}k^{-2}$)	Diffusion Coefficient (cm/sec) /Activation energy (eV)	Diffusivity @ 1000°C in Si (cm^2/sec)
~~Cs~~	~~2.14~~	~~28~~					97	3.2		
~~Rb~~	~~2.16~~	~~39~~					-	2.41		
~~K~~	~~2.3~~	~~63~~				p: Ec-0.1	83.3	2.08	1.1e-8 / 0.8	1.9e-12@800C
Sr	**2.59**	**777**	**13**	**SrS(>2000C); SrSe(1600C)**			22.5	3.6		
Ba	**2.7**	**727**	**35**	**BaSe(1780); BaN(1000)**		a: Ec-0.32; Ev+0.5	20.6	2.7		
~~Na~~	~~2.75~~	~~97~~					71	1.38	1.65e-3/ 0.72	6e-12 @800C
Ca	**2.87**	**842**	**3.4**	**Ca3N2(1195); CaSe(?)**			22.3	2.9		~6E-14
~~Li~~	~~2.9~~	~~180~~		~~**Li2Te(1204); LiSe(?)**~~		d: Ec-0.033	46	1.63	2.3e-3 / 0.66	5.60E-06
Y	**3.1**	**1526**	**56**				10.6	10.2		
La	**3.5**	**920**	**61**				12.1	10		
Sc	**3.5**	**1541**	**55**			n: Ec-0.27	10.2	10.7	8e-2 / 3.2	
~~Mg~~	~~3.66~~	~~650~~				a: Ec-0.4 d: Ec-0.115	24.8	1.3		
~~Tl~~	~~3.84~~	~~304~~			8p = 2.4e-14	p:Ev+ 0.246	29.9	1.47	16.5 / 3.9	5.80E-15
Hf	**3.9**	**2233**	**30**	**HfN(3305); HfSe2(?)**			5.9	2.16		1~3E-16
Zr	**4.05**	**1855**	**42**	**ZrN(2960); ZrSe2(?)**		d: Ec-0.07; a: Ec-0.5	5.7	2.8		2.00E-15
Mn	**4.1**	**1246**	**160**	**MnSe(1460)**	8n = 2e-14	n: EC-0.53	21.7	9.2	0.142 / 1.3	1.20E-06
~~In~~	~~4.12~~	~~156~~	~~8~~	~~InN(1100)~~	8n = 2e-15;8p = 4e-17	a: Ev+0.16	32.1	1.69	16.5 / 3.9	6.00E-15
~~Bi~~	~~4.22~~	~~271~~			Cp=6e-11(30k) Cn^+=3e-5(4.2k)	d: Ec-0.069	13.4	0.008	1030 / 4.6	4.24E-16
~~Cd~~	~~4.22~~	~~321~~	~~8~~	~~CdSe(1240)~~		a: Ev+0.55; Ec-0.45	30.8	0.688		< 1E-8
~~Pb~~	~~4.25~~					p: Ev+0.37; Ec-0.17	28.9	2.98		
Ta	**4.25**	**3017**	**13**	**TaN(3920)**	8n = 5.9e-14	n: Ec-0.232/ 0.472	6.3	5.9		
Ag	**4.26**	**961**	**1.6**	**Ag2Se(880)**		d: Ev+0.395 a: Ec-0.29	18.9	0.646	2e-5 / 1.6	9.20E-10
Al	**4.28**	**660**	**2.65**	**AlN(3000)**	Cn^o=4e-8 (4.2k)	p: Ev+0.216/ 0.316/ 0.402 n: Ec-0.389	23.1	1.35	8 / 3.47	1.42E-13
Nb	**4.3**	**2477**	**15**	**NbN(2300)**	8n = 3.6e-14	p:Ev+0.12	7.3	7.79		
V	**4.3**	**1910**	**20**	**VSe2(?)**	8n = 5e-14;8p = 8e-16	p: Ev+0.35 n: Ec-0.17	8.4	9.26		1.00E-07
Ti	**4.33**	**1668**	**40**	**TiN(3920)**	8n = 1.5e-17;8p = 3e-15	p: Ev+0.29 n: Ec-0.26	8.6	3.35	2e-5 / 1.5	2.30E-11
~~Zn~~	~~4.33~~	~~419~~	~~5.9~~	~~ZnSe(>1100)~~			30.2	0.64	0.1/ 1.4	2.80E-07
~~Sn~~	~~4.42~~	~~231~~					22	1.78	32 /4.25	4.60E-16
~~Hg~~	~~4.49~~						60.4	1.79		

Bibliography

[1] G. E. Moore, "Progress in digital integrated electronics," presented at Electron Devices Meeting, 1975 International, 1975.

[2] G. D. Wilk, R. M. Wallace, and J. M. Anthony, "High-k gate dielectrics: Current status and materials properties considerations," *Journal of Applied Physics*, vol. 89, pp. 5243-5275, 2001.

[3] B. H. Lee, L. Kang, W.-J. Qi, R. Nieh, Y. Jeon, K. Onishi, and J. C. Lee, "Ultrathin hafnium oxide with low leakage and excellent reliability for alternative gate dielectric application," presented at Electron Devices Meeting, 1999. IEDM Technical Digest. International, 1999.

[4] L. Kang, B. H. Lee, W.-J. Qi, Y. Jeon, R. Nieh, S. Gopalan, K. Onishi, and J. C. Lee, "Electrical characteristics of highly reliable ultrathin hafnium oxide gate dielectric," *Electron Device Letters, IEEE*, vol. 21, pp. 181-183, 2000.

[5] C. Hobbs, L. Fonseca, V. Dhandapani, S. Samavedam, B. Taylor, J. Grant, L. Dip, D. Triyoso, R. Hegde, D. Gilmer, R. Garcla, D. Roan, L. Lovejoy, R. Rai, L. Hebert, H. Tseng, B. White, and P. Tobin, "Fermi Level Pinning at the PolySietal Oxide Interface," *VLSI Technology Digest*, pp. 9-10, 2003.

[6] Y. C. Yeo, T. J. King, and C. M. Hu, "Metal-dielectric band alignment and its implications for metal gate complementary metal-oxide-semiconductor technology," *Journal of Applied Physics*, vol. 92, pp. 7266-7271, 2002.

[7] S. Samavedam, L. B. La, P. J. Tobin, B. White, C. Hobbs, L. R. C. Fonseca, A. Demkov, J. Schaeffer, E. Luckowski, A. Martinez, M. Raymond, D. Triyoso, D. Roan, V. Dhandapani, R. Garcia, S. G. H. Anderson, K. Moore, H. H. Tseng, C. Capasso, O. Adetutu, D. C. Gilmer, W. J. Taylor, R. Hegde, and J. Grant, "Fermi level pinning with sub-monolayer MeOx and metal gates," *IEEE Electron Device Meeting*, pp. 307-310, 2003.

[8] C. C. Hobbs, L. R. C. Fonseca, A. Knizhnik, V. Dhandapani, S. B. Samavedam, W. J. Taylor, J. M. Grant, L. G. Dip, D. H. Triyoso, R. I. Hegde, D. C. Gilmer, R. Garcia, D. Roan, M. L. Lovejoy, R. S. Rai, E. A. Hebert, H.-H. Tseng, S. G. H. Anderson, B. E. White, and P. J. Tobin, "Fermi-level pinning at the polysilicon/metal-oxide interface-Part II," *Electron Devices, IEEE Transactions on*, vol. 51, pp. 978-984, 2004.

[9] C. Hobbs, L. Fonseca, V. Dhandapani, S. Samavedam, B. Taylor, J. Grant, L. Dip, D. Triyoso, R. Hegde, D. Gilmer, R. Garcia, D. Roan, L. Lovejoy, R. Rai, L. Hebert, H. Tseng, B. White, and P. Tobin, "Fermi level pinning at the polySi/metal oxide interface," *VLSI Technology, 2003. Digest of Technical Papers. 2003 Symposium on*, pp. 9-10, 2003.

[10] C. Y. Wong, J. Y.-C. Sun, Y. Taur, C. S. Oh, R. Angelucci, and B. Davari, "Doping of n+ and p+ polysilicon in a dual-gate CMOS process," presented at

Electron Devices Meeting, 2003. IEDM '03 Technical Digest. IEEE International, 1988.

[11] J. C. Hu, H. Yang, R. Kraft, A. L. P. Rotondaro, S. Hattangady, W. W. Lee, R. A. Chapman, C.-P. Chao, A. Chatterjee, M. Hanratty, M. Rodder, and I.-C. Chen, "Feasibility of using W/TiN as metal gate for conventional 0.13 μm CMOS technology and beyond," *Electron Devices Meeting, 1997. Technical Digest., International*, pp. 825-828, 1997.

[12] ITRS, "ITRS Roadmap 2003," 2003.

[13] I. De, D. Johri, A. Srivastava, and C. M. Osburn, "Impact of gate work function on device performance at the 50 nm technology node," *Solid-State-Electronics*, vol. 44, pp. 1077-1080, 2000.

[14] E. H. Nicollian and J. R. Brews, *MOS Physics and Technology*. New york: Wiley, 1982.

[15] H. Michaelson, "The work function of the elements and its periodicity," *Journal of Applied Physics*, vol. 48, pp. 4729-4733, 1977.

[16] Y.-C. Yeo, T.-J. King, and C. Hu, "Metal-dielectric band alignment and its implications for metal gate complementary metal-oxide-semiconductor technology," *Journal of Applied Physics*, vol. 92, pp. 7266-7271, 2002.

[17] B.-Y. Tsui and C.-F. Huang, "Wide range work function modulation of binary alloys for MOSFET application," *IEEE Electron Device Letter*, vol. 24, pp. 153-155, 2003.

[18] M. A. Pawlak, T. Schram, K. Maex, and A. Vantomme, "Investigation of Iridium as a gate electrode for deep sub-micron CMOS technology," *Microelectronic Engineering*, vol. 70, pp. 373-376, 2003.

[19] B. Maiti and P. J. Tobin, "Metal Gates for Advanced CMOS Technology," *SPIE Conference on Microelectronic Device Technology III*, vol. 3881, pp. 46-57, 1999.

[20] H. Zhong, S. N. Hong, Y.-S. Suh, H. Lazar, G. Heuss, and V. Misra, "Properties of Ru-Ta alloys as gate electrodes for NMOS and PMOS silicon devices," *IEEE Electron Device Meeting*, 2001.

[21] I. Polishchuk, P. Ranade, T.-J. King, and C. Hu, "Dual work function metal gate CMOS transistors by Ni-Ti interdiffusion," *IEEE Electron Device Letter*, vol. 23, pp. 200-202, 2002.

[22] H. N. Alshareef, H. C. Wen, H. Luan, K. Choi, H. R. Harris, Y. Senzaki, P. Majhi, B. H. Lee, B. Foran, and G. Lian, "Temperature dependence of the work function of ruthenium-based gate electrodes," *Thin Solid Films*, vol. article in press Temperature dependence of the work function of ruthenium-based gate electrodes, 2006.

[23] R. Lin, Q. Lu, P. Ranade, T. J. King, and C. M. Hu, "An adjustable work function technology using Mo gate for CMOS devices," *Ieee Electron Device Letters*, vol. 23, pp. 49-51, 2002.

[24] S. H. Bae, W. P. Bai, H. C. Wen, S. Mathew, L. K. Bera, N. Balasubramanian, N. Yamada, M. F. Li, and D. L. Kwong, "Laminated metal gate electrode with tunable work function for advanced CMOS," presented at VLSI Technology, 2004. Digest of Technical Papers. 2004 Symposium on, 2004.

[25] G. Bersuker, P. Zeitzoff, J. H. Sim, B. H. Lee, R. Choi, G. Brown, and C. D. Young, "Mobility Evaluation in Transistors with Charge Trapping Gate Dielectrics," *Applied Physics Letters*, vol. 87, pp. 042905, 2005.

[26] H. N. Alshareef, H. C. Wen, H. R. Harris, K. Choi, H. F. Luan, P. Lysaght, P. Majhi, B. H. Lee, M. El-Bouanani, and V. Ukride, "Modulation of the work function of silicon gate electrode using thin TaN interlayers," *Applied Physics Letters*, vol. 87, 2005.

[27] S. Zafar, V. Narayanan, A. Callegari, F. R. McFeely, P. Jamison, E. Gusev, C. Cabral, and R. Jammy, "HfO/sub 2//metal stacks: determination of energy level diagram, work functions & their dependence on metal deposition," *VLSI Technology, 2005. Digest of Technical Papers. 2005 Symposium on*, pp. 44-45, 2005.

[28] C. C. Jr., C. Lavoie, A. S. Ozcan, R. S. Amos, V. Narayanan, E. P. Gusev, J. L. Jordam-Sweet, and J. M. E. Harper, "Evaluation of CMOS Gate Materials Using IN SITU Characterization Techniques," *Electrochemical Society Proceedings, Advanced Short-Time Thermal Processing for Si-Based CMOS Devices*, pp. 375-384, 2003.

[29] J. K. Schaeffer, S. B. Samavedam, D. C. Gilmer, V. Dhandapani, P. J. Tobin, J. Mogab, B. Y. Nguyen, B. E. White, S. Dakshina-Murthy, R. S. Rai, Z. X. Jiang, R. Martin, M. V. Raymond, M. Zavala, L. B. La, J. A. Smith, R. Garcia, D. Roan, M. Kottke, and R. B. Gregory, "Physical and electrical properties of metal gate electrodes on HfO2 gate dielectrics," *Journal of Vacuum Science & Technology B*, vol. 21, pp. 11-17, 2003.

[30] *CRC Handbook of Chemistry and Physics*, 70 ed. Boca Raton, Florida: CRC Press, Inc., 1989-1990.

[31] S. B. Samavedam, L. B. La, P. J. Tobin, B. White, C. Hobbs, L. R. C. Fonseca, A. A. Demkov, J. Schaeffer, E. Luckowski, A. Martinez, M. Raymond, D. Triyoso, D. Roan, V. Dhandapani, R. Garcia, S. G. H. Anderson, K. Moore, H. H. Tseng, C. Capasso, O. Adetutu, D. C. Gilmer, W. J. Taylor, R. Hegde, and J. Grant, "Fermi level pinning with sub-monolayer MeOx and metal gates [MOSFETs]," *Electron Devices Meeting, 2003. IEDM '03 Technical Digest. IEEE International*, pp. 13.1.1-13.1.4, 2003.

[32] J. Schaeffer, C. Capasso, L. R. C. Fonseca, S. Samavedam, L. B. La, J. Smith, S. Dakshina-Murthy, D. C. Gilmer, Luckowski, Y. Liang, S. Kalpat, B. Adetutu, H.

H. Tseng, Y. Shiho, A. Demkov, R. Hegde, W. J. Taylor, R. Gregory, J. Jiang, E. Luckowski, M. Raymond, K. Moore, D. Triyoso, D. Roan, B. White, and P. J. Tobin, "Challenges for the integration of metal gate electrodes," *IEEE Electron Device Meeting*, 2004.

[33] K. Shiraishi, Y. Akasaka, S. Miyazaki, T. Nakayama, T. Nakaoka, G. Nakamura, K. Torii, H. Furutou, A. Ohta, P. Ahmet, K. Ohmori, H. Watanabe, T. Chikyo, M. L. Green, Y. Nara, and K. Yamada, "Universal theory of workfunctions at metal/Hf-based high-k dielectrics interfaces - guiding principles for gate metal selection," *Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International*, pp. 39-42, 2005.

[34] J. K. Schaeffer, L. R. C. Fonseca, S. B. Samavedam, Y. Liang, P. J. Tobin, and B. E. White, "Contributions to the effective work function of platinum on hafnium dioxide," *Applied Physics Letters*, vol. 85, pp. 1826-1828, 2004.

[35] E. Cartier, F. R. McFeely, V. Narayanan, P. Jamison, B. P. Linder, M. Copel, V. K. Paruchuri, V. S. Basker, R. Haight, D. Lim, R. Carruthers, T. Shaw, M. Steen, J. Sleight, J. Rubino, H. Deligianni, S. Guha, R. Jammy, and G. Shahidi, "Role of oxygen vacancies in V/sub FB//V/sub t/ stability of pFET metals on HfO/sub 2/," *VLSI Technology, 2005. Digest of Technical Papers. 2005 Symposium on*, pp. 230-231, 2005.

[36] D. Gu, S. K. Dey, and P. Majhi, "Effective work function of Pt, Pd, and Re on atomic layer deposited HfO[sub 2]," *Applied Physics Letters*, vol. 89, pp. 082907, 2006.

[37] H. Yang, Y. Son, S. Baek, H. Hwang, H. Lim, and H.-S. Jung, "Ti gate compatible with atomic-layer-deposited HfO[sub 2] for n-type metal-oxide-semiconductor devices," *Applied Physics Letters*, vol. 86, pp. 092107, 2005.

[38] R. Chau, S. Datta, M. Doczy, B. Doyle, J. Kavalieros, and M. Metz, "High-K/Metal–Gate Stack and Its MOSFET Characteristics," *IEEE Electron Device Letter*, vol. 25, pp. 408-410, 2004.

[39] A. C. V. Narayanan, F.R. McFeely, K. Nakamura, P. Jamison, S. Zafar, E. Cartier, A. Steegen, V. Ku, P. Nguyen, K. Milkove, C. Cabral Jr., M. Gribelyuk, C. Wajda, Y. Kawano, D. Lacey, Y. Li, E. Sikorski, E. Duch, H. Ng, C. Wann, R. Jammy, M. Ieong, G. Shahidi, "Dual Work Function Metal Gate CMOS using CVD metal electrodes," *VLSI Technology Digest*, pp. 192-193, 2004.

[40] C. Young, G. Bersuker, H. C. Wen, G. Brown, and P. Majhi, "Charge Trapping Characteristics of Hafnium Based High-ê Dielectrics with Various Metal Electrodes," *SSDM 2004*, 2004.

[41] P. Majhi, C. Young, G. Bersuker, H. C. Wen, G. A. Brown, B. Foran, R. Choi, P. M. Zeitzoff, and H. R. Huff, "Influence of Metal Gate Materials and Processing on Planar CMOS Device Characteristics with High-k Gate Dielectrics," *ESSDERC*, 2004.

[42] http://www.intel.com/technology/mooreslaw/index.htm, "Moore's Law Means More Performance."

[43] D. V. Lang, *Thermally Stimulated Relaxation in Solids*, vol. 37. Berlin: Springer, 1979.

[44] R. Jha, J. Gurganos, Y. H. Kim, R. Choi, J. Lee, and V. Misra, "A capacitance-based methodology for work function extraction for metals on high-K," *IEEE Electron Device Letter*, vol. 25, pp. 420-423, 2004.

[45] P. Majhi, H. C. Wen, H. Alshareef, K. Choi, R. Harris, P. Lysaght, H. Luan, Y. Senzaki, S. C. Song, B. H. Lee, and C. Ramiller, "Evaluation and integration of metal gate electrodes for future generation dual metal CMOS," *Integrated Circuit Design and Technology, 2005. ICICDT 2005. 2005 International Conference on*, pp. 69-72, 2005.

[46] H. C. Wen, R. N. Choi, G. A. Brown, T. Boscke, K. Matthews, H. R. Harris, K. Choi, H. N. Alshareef, H. F. Luan, G. Bersuker, P. Majhi, D. L. Kwong, and B. H. Lee, "Comparison of effective work function extraction methods using capacitance and current measurement techniques," *Ieee Electron Device Letters*, vol. 27, pp. 598-601, 2006.

[47] J. R. Hauser and K. Ahmed, "Characterization of Ultra-Thin Oxides Using Electrical C-V and I-V Measurements," *Characterization and Metrology for ULSI Technology: 1998 International Conference*, vol. 449, pp. 235-239, 1998.

[48] G. Brown, G. Smith, J. Saulters, K. Matthews, H. C. Wen, P. Majhi, and B. H. Lee, "An Improved Methodology for Gate Electrode Work Function Extraction in SiO2 and High-k Gate Stack Systems Using Terraced Oxide Structures," *IEEE SISC conference*, 2004.

[49] H. N. Alshareef, Z. Zhang, P. Majhi, G. Brown, P. Zeitzoff, H. Huff, and B. H. Lee, "Gate electrode development for dual metal-gate CMOS applications," in *Future Fab*, vol. 19, 2005, pp. 91-93.

[50] G. D. Wilk, M. L. Green, M.-Y. Ho, B. W. Busch, T. W. Sorsch, F. P. Klemens, B. Brijs, R. B. van Dover, A. Kornblit, T. Gustafsson, E. Garfunkel, S. Hillenius, D. Monroe, P. Kalavade, and J. M. Hergenrother, "Improved film growth and flatband voltage control of ALD HfO/sub 2/ and Hf-Al-O with n/sup +/ poly-Si gates using chemical oxides and optimized post-annealing," presented at VLSI Technology, 2002. Digest of Technical Papers. 2002 Symposium on, 2002.

[51] C. C. Hobbs, L. .Fonseca, A. Knizhnik, V. Dhandapani, S. B. Samavedam, W. J. Taylor, J. M. Grant, L. G. Dip, D. H. Triyoso, R. I. Hegde, D. C. Gilmer, R. Garcia, D. Roan, M. L. Lovejoy, R. S. Rai, E. A. Hebert, H.-H. Tseng, S. G. H. Anderson, B. E. White, and P. J. Tobin, "Fermi-Level Pinning at the Polysilicon/Metal–Oxide Interface—Part II," *IEEE Transactions on Electron Devices*, vol. 51, pp. 978-984, 2004.

[52] S. Zafar, C. Cabral, A. R., and A. Callegari, "A method for measuring barrier heights, metal work functions and fixed charge densities in metal/SiO2/Si capacitors," *Applied Physics Letters*, vol. 80, pp. 4858-4860, 2002.

[53] S. Zafar, E. Cartier, and E. P. Gusev, "Measurement of barrier heights in high permittivity gate dielectric films," *Applied Physics Letters*, vol. 80, pp. 2749-2751, 2002.

[54] T. Hori, *Gate Dielectrics and MOS ULSI Principles, Technologies and Application*: Springer-Verlag Berlin Heidelberg, 1997.

[55] J. Robertson, "Band offsets of wide-band-gap oxides and implications for future electronic devices," presented at Papers from the international conference on silicon dielectric interfaces, 2000.

[56] A. A. Demkov, L. R. C. Fonseca, E. Verret, J. Tomfohr, and O. F. Sankey, "Complex band structure and the band alignment problem at the Si--high-k dielectric interface," *Physical Review B (Condensed Matter and Materials Physics)*, vol. 71, pp. 195306, 2005.

[57] A. S. Grove, *Physics and Technology of Semiconductor Devices*. New York: Wiley, 1967.

[58] P. Majhi, H.-C. Wen, K. Choi, H. Alshareef, C. Huffman, and B. H. Lee, "A systematic study of the influence of nitrogen in tuning the effective work function of nitrided metal gates," presented at VLSI Technology, 2005. (VLSI-TSA-Tech). 2005 IEEE VLSI-TSA International Symposium on, 2005.

[59] C. Ren, H. Y. Yu, J. F. Kang, Y. T. Hou, M. E. Li, W. D. Wang, D. S. H. Chan, and D. L. Kwong, "Fermi-level pinning induced thermal instability in the effective work function of TaN in TaN/SiO2 gate stack," *Ieee Electron Device Letters*, vol. 25, pp. 123-125, 2004.

[60] Y. C. Yeo, P. Ranade, T. J. King, and C. M. Hu, "Effects of high-kappa gate dielectric materials on metal and silicon gate workfunctions," *Ieee Electron Device Letters*, vol. 23, pp. 342-344, 2002.

[61] H. Y. Yu, C. Ren, Y. C. Yeo, J. F. Kang, X. P. Wang, H. H. H. Ma, M. F. Li, D. S. H. Chan, and A. L. Kwong, "Fermi pinning-induced thermal instability of metal-gate work functions," *Ieee Electron Device Letters*, vol. 25, pp. 337-339, 2004.

[62] Y. Liang, J. Curless, C. J. Tracy, D. C. Gilmer, J. K. Schaeffer, D. H. Triyoso, and P. J. Tobin, "Interface dipole and effective work function of Re in Re/HfO[sub 2]/SiO[sub x]/n-Si gate stack," *Applied Physics Letters*, vol. 88, pp. 072907, 2006.

[63] M. Copel, R. P. Pezzi, D. Neumayer, and P. Jamison, "Reduction of hafnium oxide and hafnium silicate by rhenium and platinum," *Applied Physics Letters*, vol. 88, pp. 072914, 2006.

[64] L. Pantisano, T. Schram, Z. Li, J. G. Lisoni, G. Pourtois, S. D. Gendt, D. P. Brunco, A. Akheyar, V. V. Afanas'ev, S. Shamuilia, and A. Stesmans, "Ruthenium gate electrodes on SiO[sub 2] and HfO[sub 2]: Sensitivity to hydrogen and oxygen ambients," *Applied Physics Letters*, vol. 88, pp. 243514, 2006.

[65] H. C. Wen, P. Lysaght, H. N. Alshareef, C. Huffman, H. R. Harris, K. Choi, Y. Senzaki, H. Luan, P. Majhi, B. H. Lee, M. J. Campin, B. Foran, G. D. Lian, and D. L. Kwong, "Thermal response of Ru electrodes in contact with SiO2 and Hf-based high-k gate dielectrics," *Journal of Applied Physics*, vol. 98, 2005.

[66] H.-C. Wen, K. Choi, P. Majhi, H. Alshareef, C. Huffman, and B. H. Lee, "A systematic study of the influence of nitrogen in tuning the effective work function of nitrided metal gates," presented at VLSI Technology, 2005. (VLSI-TSA-Tech). 2005 IEEE VLSI-TSA International Symposium on, 2005.

[67] J. Robertson, "Invited talk at EMRS 2006," 2006.

[68] G. Pant, A. Gnade, M. J. Kim, R. M. Wallace, B. E. Gnade, M. A. Quevedo-Lopez, and P. D. Kirsch, "Effect of thickness on the crystallization of ultrathin HfSiON gate dielectrics," *Applied Physics Letters*, vol. 88, pp. 032901, 2006.

[69] *Diagrammy Sostoianiia Metallicheskikh sistem, Moscow*, 1971.

[70] V. Misra, H. C. Zhong, and H. Lazar, "Electrical properties of Ru-based alloy gate electrodes for dual metal gate Si-CMOS," *Ieee Electron Device Letters*, vol. 23, pp. 354-356, 2002.

[71] H. C. Wen, K. Choi, P. Lysaght, P. Majhi, H. Alshareef, C. Huffman, R. Harris, H. Luan, B. H. Lee, N. Yamada, and S. Wickramanayaka, "Work function engineering of RuHf alloys as gate electrodes for future generation dual metal CMOS," presented at VLSI Technology, 2005. (VLSI-TSA-Tech). 2005 IEEE VLSI-TSA International Symposium on, 2005.

[72] H. Y. Yu, M. F. Li, and D. L. Kwong, "Thermally robust HfN metal as a promising gate electrode for advanced MOS device applications," *Ieee Transactions on Electron Devices*, vol. 51, pp. 609-615, 2004.

[73] J. Westlinder, G. Sjoblom, and J. Olsson, "Variable work function in MOS capacitors utilizing nitrogen-controlled TiNx gate electrodes," *Microelectronic Engineering*, vol. 75, pp. 389-396, 2004.

[74] W. Gordy and W. J. O. Thomas, "Electronegativities of the Elements," *The Journal of Chemical Physics*, vol. 24, pp. 439-444, 1956.

[75] J. Schaeffer, D. Gilmer, S. Samavedam, D. Triyoso, R. Hegde, S. Kalpat, M. Raymond, C. Capasso, B. Taylor, M. Sadd, H. H. Tseng, M. Stoker, A. Haggag, D. Roan, L. L. Happ, C. , P. J. Tobin, and B. E. White, "Materials Challenges for High Permittivity Gate Dielectrics and Metal Gate Electrodes," *IEEE ISAGST 2006*, 2006.

[76] M.-A. Nicolet and P. H. Giauque, "Highly metastable amorphous or near-amorphous ternary films (mictamict alloys)," *Microelectronic Engineering*, vol. 55, pp. 357-367, 2001.

[77] Y. S. Suh, G. P. Heuss, J. H. Lee, and V. Misra, "Effect of the composition on the electrical properties of TaSixNy metal gate electrodes," *Ieee Electron Device Letters*, vol. 24, pp. 439-441, 2003.

[78] T. Hori, *Gate dielectrics and MOS ULSIs: Principles, Technologies and Applications*. Germany: Springer.

[79] W.-H. Lee, J. T. Clemens, R. C. Keller, and L. Manchanda, "A Novel High K Inter-poly Dielectric(IPD), A1/sub 2/O/sub 3/ For Low Voltage/high Speed Flash memories: erasing in msecs at 3.3V," presented at VLSI Technology, 1997. Digest of Technical Papers., 1997 Symposium on, 1997.

[80] W. S. Yang, Y. K. Kim, S. U. Yang, J. H. Choi, H. S. Park, S. I. Lee, and J. B. Yoo, "Effect of SiO2 inermediate on Al2O3 and SiO2 n-poly Si interface deposited using atomic layer deposition (ALD) for deep submicron device applications," *Surface and coatings technology*, vol. 131, pp. 79-83, 2000.

[81] S. H. Bae, C. H. Lee, R. Clark, and D. L. Kwong, "MOS Characteristics of Ultrathin CVD HfAlO Gate Dielectrics," *IEEE Electron Device Letters*, vol. 24, pp. 556~558, 2003.

[82] R. S. Johnson, G. Lucovsky, and I. Baumvol, "Physical and electrical properties of noncrystalline Al2O3 prepared by remote plasma enhanced chemical vapor deposition," *J. Vac. Sci. Technol. A*, vol. 19, pp. 1353-1360, 2001.

[83] H. N. Alshareef, H. F. Luan, K. Choi, H. R. Harris, H. C. Wen, M. A. Quevedo-Lopez, P. Majhi, and B. H. Lee, "Metal gate work function engineering using AlN[sub x] interfacial layers," *Applied Physics Letters*, vol. 88, pp. 112114, 2006.

[84] H.-S. Jung, *VLSI Technology, 2006. Digest of Technical Papers. 2006 Symposium on*, 2006.

[85] K. Lee, M. Frank, V. Paruchuri, E. Cartier, B. Linder, N. Bojarczuk, X. Wang, J. Rubino, M. Steen, P. Kozlowski, J. Newbury, E. Sikorski, P. Flaitz, M. Gribelyuk, P. Jamison, G. Singco, V. Narayanan, S. Zafar, S. Guha, P. Oldiges, R. Jammy, and M. Ieong, "Poly-Si/AlN/HfSiO Stack for Ideal Threshold Voltage and Mobility in Sub-100 nm MOSFETs," presented at VLSI Technology, 2006. Digest of Technical Papers. 2006 Symposium on, 2006.

[86] T. H. Cha, D. G. Park, T. K. Kim, S. A. Jang, I. S. Yeo, J. S. Roh, and J. W. Park, "Work function and thermal stability of Ti1-xAlxNy for dual metal gate electrodes," *Applied Physics Letters*, vol. 81, pp. 4192-4194, 2002.

[87] H. N. Alshareef, K. Choi, H. C. Wen, H. Luan, H. Harris, Y. Senzaki, P. Majhi, B. H. Lee, R. Jammy, S. Aguirre-Tostado, B. E. Gnade, and R. M. Wallace, "Composition dependence of the work function of Ta[sub 1 - x]Al[sub x]N[sub y] metal gates," *Applied Physics Letters*, vol. 88, pp. 072108, 2006.

[88] J. C. Schuster and H. Nowotny, "Phase relationships in the ternary systems (V, Cr, Mo, W, Mn, Re)-Al-N," *Journal of Materials Science*, vol. 20, pp. 2787-2793, 1985.

[89] H. Alshareef, H. Harris, H. Wen, C. Park, C. Huffman, K. Choi, H. Luan, P. Majhi, B. Lee, R. Jammy, D. Lichtenwalner, J. Jur, and A. Kingon, "Thermally Stable N-Metal Gate MOSFETs Using La-Incorporated HfSiO Dielectric," *VLSI Technology, 2006. Digest of Technical Papers. 2006 Symposium on*, pp. 7-8, 2006.

[90] H. Ono, *Applied Physics Letters*, vol. 78, pp. 1832, 2001.

[91] N. Kimizuka, *VLSI Technology, 1999. Digest of Technical Papers*, pp. 73, 1999.

[92] L. Pantisano, T. Schram, B. O'Sullivan, T. Conard, S. D. Gendt, G. Groeseneken, P. Zimmerman, A. Akheyar, M. M. Heyns, S. Shamuilla, V. V. Afanas'ev, and A. Stesmans, "Effective work function modulation by controlled dielectric monolayer deposition," *Applied Physics Letters*, vol. 89, pp. 113505, 2006.

[93] V. Narayanan, V. Paruchuri, N. Bojarczuk, B. Linder, B. Doris, Y. Kim, S. Zafar, J. Stathis, S. Brown, J. Arnold, M. Copel, M. Steen, E. Cartier, A. Callegari, P. Jamison, J.-P. Locquet, D. Lacey, Y. Wang, P. Batson, P. Ronsheim, R. Jammy, and M. Chudzik, "Band-Edge High-Performance High-k/Metal Gate n-MOSFETs Using Cap Layers Containing Group IIA and IIIB Elements with Gate-First Processing for 45 nm and Beyond," *VLSI Technology, 2006. Digest of Technical Papers. 2006 Symposium on*, pp. 178-179, 2006.

[94] Y. Yamamoto, K. Kita, K. Kyuno, and A. Toriumi, "Study of La concentration dependent Vfb shift in metal/HfLaOx/Si capacitors," *International Conference on Solid State Devices and Materials 2006*, pp. 212, 2006.

[95] R. Chau, S. Datta, M. Doczy, B. Doyle, J. Kavalieros, and M. Metz, "High-kappa/metal-gate stack and its MOSFET characteristics," *Ieee Electron Device Letters*, vol. 25, pp. 408-410, 2004.

[96] D.-G. Park, Z. J. Luo, N. Edleman, W. Zhu, P. Nguyen, K. Wong, C. Cabral, P. Jamison, B. H. Lee, A. Chou, M. Chudzik, J. Bruley, O. Gluschenkov, P. Ronsheim, A. Chakravarti, R. Mitchell, V. Ku, H. Kim, E. Duch, P. Kozlowski, C. D'Emic, V. Narayanan, A. Steegen, R. Wise, R. Jammy, R. Rengarajan, H. Ng, A. Sekiguchi, and C. H. Wann, "Thermally robust dual-work function ALD-MNx MOSFETs using conventional CMOS process flow," *VLSI Technology Digest*, 2004.

[97] S. M. Sze, *Physics of Semiconductor Devices*: John Wiley & Sons Inc., 1981.

[98] Y. Ma, L. Liu, and Z. Li, "A discussion on the universality of inversion layer mobility in MOSFET's," *Electron Devices, IEEE Transactions on*, vol. 46, pp. 1920-1922, 1999.

[99] P. D. Kirsch, M. A. Quevedo-Lopez, S. A. Krishnan, C. Krug, H. AlShareef, C. S. Park, R. Harris, N. Moumen, A. Neugroschel, G. Bersuker, B. H. Lee, J. G.

Wang, G. Pant, B. E. Gnade, M. J. Kim, R. M. Wallace, J. S. Jur, D. J. Lichtenwalner, A. I. Kingon, and R. Jammy, "Band Edge n-MOSFETs with High-k/Metal Gate Stacks Scaled to EOT=0.9nm with Excellent Carrier Mobility and High Temperature Stability," *Electron Devices Meeting, 2006*, pp. s23p4, 2006.

[100] W. Zhu, J.-P. Han, and T. P. Ma, "Mobility measurement and degradation mechanisms of MOSFETs made with ultrathin high-k dielectrics," *Electron Devices, IEEE Transactions on*, vol. 51, pp. 98-105, 2004.

[101] G. Bersuker, J. H. Sim, C. D. Young, R. Choi, B. H. Lee, P. Lysaght, G. Brown, P. Zeitzoff, M. Gardner, R. W. Murto, and H. R. Huff, "Effect of structural properties of Hf-based gate stack on transistor performance," *Materials Research Society Symposium*, vol. 811, pp. 31, 2004.

[102] J. L. Gavartin, A. L. Shluger, A. S. Foster, and G. Bersuker, "The role of nitrogen-related defects in high-K dielectric oxides: Density-functional studies," *Journal of Applied Physics*, vol. 97, pp. 053704-1~12, 2005.

[103] P. D. Kirsch, J. H. Sim, S. C. Song, S. Krishnan, J. Peterson, H. J. Li, M. Quevedo-Lopez, C. D. Young, R. Choi, N. Moumen, P. Majhi, Q. Wang, J. G. Ekerdt, G. Bersuker, and B. H. Lee, "Mobility enhancement of high-k gate stacks through reduced transient charging," *Solid-State Device Research Conference, 2005. ESSDERC 2005. Proceedings of 35th European*, pp. 367-370, 2005.

[104] M. Koike, T. Ino, Y. Kamimuta, M. Koyama, Y. Kamata, M. Suzuki, Y. Mitani, A. Nishiyama, and Y. Tsunashima, "Effect of Hf-N bond on properties of thermally stable amorphous HfSiON and applicability of this material to sub-50nm technology node LSIs," *Electron Devices Meeting, 2003. IEDM '03 Technical Digest. IEEE International*, pp. 4.7.1-4.7.4, 2003.

[105] M. A. Quevedo-Lopez, S. A. Krishnan, P. D. Kirsch, H. J. Li, J. H. Sim, C. Huffman, J. J. Peterson, B. H. Lee, G. Pant, B. E. Gnade, M. J. Kim, R. M. Wallace, D. Guo, H. Bu, and T. P. Ma, "High Performance Gate First HfSiON Dielectric Satisfying 45nm Node Requirements," *IEEE Electron Device Meeting*, vol. 17.4, 2005.

[106] Y. Akasaka, K. Miyagawa, T. Sasaki, K. Shiraishi, S. Kamiyama, O. Ogawa, F. Ootsuka, and Y. Nara, "Impact of electrode-side chemical structures on electron mobility in metal/HfO/sub 2/ MISFETs with sub-1nm EOT," *VLSI Technology, 2005. Digest of Technical Papers. 2005 Symposium on*, pp. 228-229, 2005.

[107] J. R. Hauser, "Extraction of experimental mobility data for MOS devices," *Electron Devices, IEEE Transactions on*, vol. 43, pp. 1981-1988, 1996.

[108] T. Yamaguchi, R. Iijima, T. Ino, A. Nishiyama, H. Satake, and N. Fukushima, ="Additional scattering effects for mobility degradation in Hf-silicate gate MISFETs," *IEEE Electron Device Meeting*, vol. Technology Digest, pp. 621-624, 2002.

[109] C. D. Young, R. Choi, J. H. Sim, B. H. Lee, P. Zeitzoff, Y. Zhao, K. Matthews, G. A. Brown, and G. Bersuker, "Interfacial layer dependence of HFSI/sub x/O/sub y/ gate stacks on V/sub T/ instability and charge trapping using ultra-short pulse in characterization," *Reliability Physics Symposium, 2005. Proceedings. 43rd Annual. 2005 IEEE International*, pp. 75-79, 2005.

[110] C. D. Young, P. Zeitzoff, G. A. Brown, G. Bersuker, B. H. Lee, and J. R. Hauser, "Intrinsic mobility evaluation of high-/spl kappa/ gate dielectric transistors using pulsed I/sub d/-V/sub g/," *Electron Device Letters, IEEE*, vol. 26, pp. 586-589, 2005.

[111] A. Kerber, E. Cartier, L. A. Ragnarsson, M. Rosmeulen, L. Pantisano, R. Degraeve, Y. Kim, and G. Groesenenken, "Direct measurment of the inversion charge in MOSFETs: Application to mobility extraction in alternative gate dielectrics," *VLSI Symosium Tech. Dig.*, pp. 159-160, 2003.

[112] C. D. Young, S. Nadkarni, D. Heh, H. R. Harris, R. Choi, J. Peterson, J. H. Sim, S. Krishnan, J. Barnett, E. Vogel, B. H. Lee, P. Zeitzoff, G. Brown, and G. Bersuker, "Detection of electron trap generation due to constant voltage stress on high-K gate stacks," *International reliability physics symposium*, vol. 3.A.1, 2006.

[113] G. Bersuker, B. H. Lee, H. R. Huff, J. Gavartin, and A. Shluger, "Mechanism of charge trapping reduction in scaled high-K gate stacks," presented at Proceedings of the NATO Advanced Research Workshop on Defects in Advanced High-K Dielectric Nano-Electronic Semiconductor Devices, St. Petersburg, Russia, 2006.

[114] C. D. Young, G. Bersuker, Y. Zhao, J. Peterson, J. Barnett, G. Brown, J. H. Sim, R. Choi, B. H. Lee, and P. Zeitzoff, "Probing stress effects in HfO2 gate stacks with time dependent measurements," *Microelectronics Reliability*, vol. 45, pp. 806-810, 2005.

[115] R. Degraeve, A. Kerber, E. Cartier, L. Pantisano, and G. Groesenenken, "Effect of bulk trap density on HfO2 reliability and yield," *IEEE Electron Device Meeting*, pp. 935-938, 2003.

[116] V. Misra, G. P. Heuss, and Z. H., "Use of metal-oxide-semiconductor capacitors to detect interactions of Hf and Zr gate electrodes with SiO2 and ZrO2," *Applied Physics Letters*, vol. 78, pp. 4166-4168, 2001.

[117] C. Choi, C. Y. Kang, S. J. Rhee, M. Akbar, S. Krishnan, M. Zhang, H. Kim, T. Lee, I. Ok, F. Zhu, and J. C. Lee, "Aggressively scaled ultra thin undoped HfO2 gate dielectric (EOT<0.7nm) with TaN gate electrode using engineered interface layer," *IEEE Electron Device Letters*, vol. 26, pp. 454-456, 2005.

[118] L. V. Goncharova, M. Dalponte, D. G. Starodub, T. Gustafsson, E. Garfunkel, P. S. Lysaght, B. F. Barnett, and G. I. Bersuker, "Oxygen diffusion and reactions in Hf-based dielectrics," *Applied Physics Letters*, vol. 89, pp. 044108, 2006.

[119] J. H. Sim, S. C. Song, P. D. kirsch, C. D. Young, R. Choi, D. L. Kwong, B. H. Lee, and G. Bersuker, "Effects of ALD HfO2 thickness on charge trapping and mobility," *Insulating films on semiconductors INFOS 2005*, pp. 8.1, 2005.

[120] S. A. Krishnan, M. Quevedo, R. Harris, P. D. Kirsch, R. Choi, B. H. Lee, G. Bersuker, J. Peterson, H.-J. Li, C. D. Young, and J. C. Lee, "NBTI Dependence on Dielectric Thickness in Ultra-scaled HfSiO Dielectric/ ALD-TiN Gate Stacks," *2005 International conference on SOLID STATE DEVICES AND MATERIALS*, pp. A.2-4, 2005.

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[1] H. C. Wen, R. N. Choi, G. A. Brown, T. Boscke, K. Matthews, H. R. Harris, K. Choi, H. N. Alshareef, H. F. Luan, G. Bersuker, P. Majhi, D. L. Kwong, and B. H. Lee, "Comparison of effective work function extraction methods using capacitance and current measurement techniques," *Ieee Electron Device Letters*, vol. 27, pp. 598-601, 2006.

[2] H.-C. Wen, H. R. Harris, C. Young, H. Luan, H. Alshareef, K. Choi, D. L. Kwong, P. Majhi, G. Bersuker, and B. H. Lee, "On oxygen deficiency and fast transient charge trapping effects in high-K dielectrics," *Ieee Electron Device Letters*, 2006.

[3] H. C. Wen, P. Lysaght, H. N. Alshareef, C. Huffman, H. R. Harris, K. Choi, Y. Senzaki, H. Luan, P. Majhi, B. H. Lee, M. J. Campin, B. Foran, G. D. Lian, and D. L. Kwong, "Thermal response of Ru electrodes in contact with SiO2 and Hf-based high-k gate dielectrics," *Journal of Applied Physics*, vol. 98, 2005.

[4] H. C. Wen, J. H. Sim, J. P. Lu, and D. L. Kwong, "Effect of Ni thickness dependence on NiSiFUSI metal gate characteristics," *Electrochemical and Solid State Letters*, vol. 7, pp. G258-G260, 2004.

[5] H. C. Wen, J. Liu, J. H. Sim, J. P. Lu, and D. L. Kwong, "Investigation of dopant effects in CoSi2 and NiSi fully silicided metal gates," *Electrochemical and Solid State Letters*, vol. 8, pp. G119-G121, 2005.

[6] J. H. Sim, H. C. Wen, J. P. Lu, and D. L. Kwong, "Dual work function metal gates using full nickel silicidation of doped poly-Si," *Electron Device Letters, IEEE*, vol. 24, pp. 631-633, 2003.

[7] J. H. Sim, H. C. Wen, J. P. Lu, and D. L. Kwong, "Dual work function metal gates using full nickel silicidation of doped poly-Si," *Ieee Electron Device Letters*, vol. 24, pp. 631-633, 2003.

[8] K. Choi, H. N. Alshareef, H. C. Wen, H. Harris, H. Luan, Y. Senzaki, P. Lysaght, P. Majhi, and B. H. Lee, "Effective work function modification of atomic-layer-deposited-TaN film by capping layer," *Applied Physics Letters*, vol. 89, 2006.

[9] K. Choi, P. Lysaght, H. Alshareef, C. Huffman, H. C. Wen, R. Harris, H. Luan, P. Y. Hung, C. Sparks, M. Cruz, K. Matthews, P. Majhi, and B. H. Lee, "Growth mechanism of TiN film on dielectric films and the effects on the work function," *Thin Solid Films*, vol. 486, pp. 141-144, 2005.

[10] J. Liu, H. C. Wen, J. P. Lu, and D. L. Kwong, "Dual-work-function metal gatesby full silicidation of poly-Si with Co-NiBi-layers," *Ieee Electron Device Letters*, vol. 26, pp. 228-230, 2005.

[11] G. Thareja, H. C. Wen, R. Harris, P. Majhi, B. H. Lee, and J. C. Lee, "NMOS Compatible Work Function of TaN Metal Gate With Gadolinium Oxide Buffer Layer on Hf-Based Dielectrics," *Electron Device Letters, IEEE*, vol. 27, pp. 802-804, 2006.

[12] H. N. Alshareef, H. C. Wen, H. R. Harris, K. Choi, H. F. Luan, P. Lysaght, P. Majhi, B. H. Lee, M. El-Bouanani, and V. Ukride, "Modulation of the work function of silicon gate electrode using thin TaN interlayers," *Applied Physics Letters*, vol. 87, 2005.

[13] J. Liu, H. C. Wen, J. P. Lu, and D. L. Kwong, "Improving gate-oxide reliability by TiN capping layer on NiSi FUSI metal gate," *Electron Device Letters, IEEE*, vol. 26, pp. 458-460, 2005.

[14] J. Liu, H. C. Wen, J. P. Lu, and D. L. Kwong, "The impact of TiN capping layer on NiSi, COSi2, and CoxNi1-xSi2FUSI metal gate work function adjustment," *Ieee Transactions on Electron Devices*, vol. 52, pp. 2703-2709, 2005.

[15] W. P. Bai, S. H. Bae, H. C. Wen, S. Mathew, L. K. Bera, N. Balasubramanian, N. Yamada, M. F. Li, and D.-L. Kwong, "Three-Layer laminated metal gate electrodes with tunable work functions for CMOS applications," *Electron Device Letters, IEEE*, vol. 26, pp. 231-233, 2005.

[16] H. N. Alshareef, H. C. Wen, H. Luan, K. Choi, H. R. Harris, Y. Senzaki, P. Majhi, B. H. Lee, B. Foran, and G. Lian, "Temperature dependence of the work function of ruthenium-based gate electrodes," *Thin Solid Films*, vol. article in press Temperature dependence of the work function of ruthenium-based gate electrodes, 2006.

[17] H. Luan, H. N. Alshareef, H. R. Harris, H. C. Wen, K. Choi, Y. Senzaki, P. Majhi, and B. H. Lee, "Evaluation of titanium silicon nitride as gate electrodes for complementary metal-oxide semiconductor," *Applied Physics Letters*, vol. 88, 2006.

[18] H. N. Alshareef, K. Choi, H. C. Wen, H. Luan, H. Harris, Y. Senzaki, P. Majhi, B. H. Lee, R. Jammy, S. Aguirre-Tostado, B. E. Gnade, and R. M. Wallace, "Composition dependence of the work function of Ta1-xAlxNy metal gates," *Applied Physics Letters*, vol. 88, 2006.

[19] H. N. Alshareef, H. F. Luan, K. Choi, H. R. Harris, H. C. Wen, M. A. Quevedo-Lopez, P. Majhi, and B. H. Lee, "Metal gate work function engineering using AlNx interfacial layers," *Applied Physics Letters*, vol. 88, 2006.

[20] H. Luan, H. N. Alshareef, P. S. Lysaght, H. R. Harris, H. C. Wen, K. Choi, Y. Senzaki, P. Majhi, and B. H. Lee, "Evaluation of tantalum silicon alloy systems as gate electrodes," *Applied Physics Letters*, vol. 87, 2005.

[21] T. Y. Chang, T. F. Lei, T. S. Chao, H. C. Wen, and H. W. Chen, "Improvement of low-temperature gate dielectric formed in N2O plasma by an additional CF4 pretreatment process," *Ieee Electron Device Letters*, vol. 23, pp. 389-391, 2002.

[22] T. Y. Chang, J. W. Lee, T. F. Lei, C. L. Lee, and H. C. Wen, "Growing high-performance tunneling oxide by CF4 plasma pretreatment," *Journal of the Electrochemical Society*, vol. 150, pp. G33-G38, 2003.

[23] H. C. Wen, P. Lysaght, M. J. Campin, B. Foran, C. Huffman, H. N. Alshareef, K. Choi, and P. Majhi, "Thermal Response of Ru Electrodes in Contact with SiO2 and HfSiOx Gate Dielectrics," presented at Materials Reserach Society Symposium, 2004.

[24] H. C. Wen, H. N. Alshareef, H. Luan, K. Choi, P. Lysaght, H. R. Harris, C. Huffman, G. A. Brown, G. Bersuker, P. Zeitzoff, H. Huff, P. Majhi, and B. H. Lee, "Systematic investigation of amorphous transition-metal-silicon-nitride electrodes for metal gate CMOS applications," *VLSI Technology, 2005. Digest of Technical Papers. 2005 Symposium on*, pp. 46-47, 2005.

[25] H. C. Wen, K. Choi, P. Lysaght, P. Majhi, H. Alshareef, C. Huffman, R. Harris, H. Luan, B. H. Lee, N. Yamada, and S. Wickramanayaka, "Work function engineering of RuHf alloys as gate electrodes for future generation dual metal CMOS," presented at VLSI Technology, 2005. (VLSI-TSA-Tech). 2005 IEEE VLSI-TSA International Symposium on, 2005.

[26] K. Choi, P. Lysaght, H.-C. Wen, K. Matthews, H. Alshareef, C. Huffman, R. Harris, H. Luan, P. Majhi, and B. H. Lee, "Growth mechanism of ALD-TiN and the thickness dependence of work function," presented at VLSI Technology, 2005. (VLSI-TSA-Tech). 2005 IEEE VLSI-TSA International Symposium on, 2005.

[27] P. S. Lysaght, H.-C. Wen, H. Alshareef, K. Choi, R. Harris, H. Luan, Y. Senzaki, G. Lian, M. Campin, M. Clark, B. Foran, P. Majhi, and B.-H. Lee, "Physical Characterization of Novel Metal Electrodes for Hf-based Transistors," presented at CHARACTERIZATION AND METROLOGY FOR ULSI TECHNOLOGY 2005, Richardson, Texas (USA), 2005.

[28] H. Alshareef, H. Harris, H. Wen, C. Park, C. Huffman, K. Choi, H. Luan, P. Majhi, B. Lee, R. Jammy, D. Lichtenwalner, J. Jur, and A. Kingon, "Thermally Stable N-Metal Gate MOSFETs Using La-Incorporated HfSiO Dielectric," presented at VLSI Technology, 2006. Digest of Technical Papers. 2006 Symposium on, 2006.

[29] H. R. Harris, H. C. Wen, K. Choi, H. Alshareef, H. Luan, Y. Senzaki, C. D. Young, S. C. Song, Z. Zhang, G. Bersuker, P. Majhi, and B. H. Lee, "Demonstration of high performance transistors with PVD metal gate," *Solid-State Device Research Conference, 2005. ESSDERC 2005. Proceedings of 35th European*, pp. 431-434, 2005.

[30] K. Choi, H.-C. Wen, H. Alshareef, R. Harris, P. Lysaght, H. Luan, P. Majhi, and B. H. Lee, "The effect of metal thickness, overlayer and high-k surface treatment on the effective work function of metal electrode," presented at Solid-State Device Research Conference, 2005. ESSDERC 2005. Proceedings of 35th European, 2005.

[31] P. Majhi, H. C. Wen, H. Alshareef, K. Choi, R. Harris, P. Lysaght, H. Luan, Y. Senzaki, S. C. Song, B. H. Lee, and C. Ramiller, "Evaluation and integration of metal gate electrodes for future generation dual metal CMOS," *Integrated Circuit Design and Technology, 2005. ICICDT 2005. 2005 International Conference on*, pp. 69-72, 2005.

[32] B. H. Lee, H. C. Wen, H. Harris, S. C. Song, K. Choi, P. Kirsch, P. Majhi, and R. Jammy, "Advances and Challenges in Gate Stack Technology for Nano Scale CMOS Devices," presented at 7th International Conference on Microelectronics and Interfaces, Austin, Texas, 2006.

[33] P. Majhi, H. C. Wen, G. Bersuker, G. Brown, B. H. Lee, and H. Huff, "Advanced gate electrodes for future generation CMOS," in *Semiconductor FABTECH*, 2004, pp. 122-127.

[34] S. H. Bae, W. P. Bai, H. C. Wen, S. Mathew, L. K. Bera, N. Balasubramanian, N. Yamada, M. F. Li, and D. L. Kwong, "Laminated metal gate electrode with tunable work function for advanced CMOS," *VLSI Technology Digest*, 2004.

[35] P. Majhi, C. Young, G. Bersuker, H. C. Wen, G. A. Brown, B. Foran, R. Choi, P. M. Zeitzoff, and H. R. Huff, "Influence of metal gate materials and processing on planar CMOS device characteristics with high-k gate dielectrics," presented at Solid-State Device Research conference, 2004. ESSDERC 2004. Proceeding of the 34th European, 2004.

[36] G. Brown, G. Smith, J. Saulters, K. Matthews, H. C. Wen, P. Majhi, and B. H. Lee, "An Improved Methodology for Gate Electrode Work Function Extraction in SiO2 and High-k Gate Stack Systems Using Terraced Oxide Structures," *IEEE SISC conference*, 2004.

[37] C. Young, G. Bersuker, H. C. Wen, G. Brown, and P. Majhi, "Charge Trapping Characteristics of Hafnium Based High-ê Dielectrics with Various Metal Electrodes," *SSDM 2004*, 2004.

[38] B. H. Lee, C. D. Young, R. Choi, J. H. Sim, G. Bersuker, C. Y. Kang, R. Harris, G. A. Brown, K. Matthews, S. C. Song, N. Moumen, J. Barnett, P. Lysaght, K. S. Choi, H. C. Wen, C. Huffman, H. Alshareef, P. Majhi, S. Gopalan, J. Peterson, P. Kirsh, H.-J. Li, J. Gutt, M. Gardner, H. R. Huff, P. Zeitzoff, R. W. Murto, L. Larson, and C. Ramiller, "Intrinsic characteristics of high-k devices and implications of fast transient charging effects (FTCE)," presented at Electron Devices Meeting, 2004. IEDM Technical Digest. IEEE International, 2004.

[39] S. C. Song, B. Lee, Z. Zhang, K. Choi, S. H. Bae, H. Alshareef, P. Majhi, H. Wen, J. Bennett, B. Sassman, and P. Zeitzoff, "Comparision of MOSFET Characteristics Between ALD and MOCVD TiN Metal Gate on Hf Silicate," presented at 207th ECS Meeting, Quebec City, Canada, 2005.

[40] P. Majhi, H. Wen, K. Choi, P. Lysaght, C. Huffman, H. Luan, H. Harris, B. Lee, and C. Ramiller, "On the Structure-Property Inter-Relationships of Metal Gate Electrodes for Future Generation CMOS," presented at ECS ISTC, Shanghai, China, 2005.

[41] H. Alshareef, K. Choi, H. C. Wen, H. Harris, H. Luan, P. Lysaght, P. Majhi, and B. H. Lee, "Gate Work Function Modification Using Ultra-Thin Metal Interlayers," presented at 207th ECS meeting, Quebec City, Canada, 2005.

[42] K. Choi, Y. Senzaki, H. Luan, H. Alshareef, H. Harris, H. Wen, C. Park, P. Majhi, and B. H. Lee, "N-type band edge work function demonstration employing plasma-enhanced ALD HfSiN gate electrodes on high-k dielectrics," presented at AVS 5th International Conference on Atomic Layer Deposition, San Jose, California, 2005.

[43] G. Thareja, S. J. Rhee, H. C. Wen, H. Harris, P. Majhi, B. H. Lee, and J. C. Lee, "Low Work-Function TaN-metal gate with Gadolinium Oxide Buffer Layer on Hf-based Dielectrics," presented at IEEE Device Research Conference, University Park, PA, 2006.

[44] H. Harris, S. Krishnan, H. C. Wen, H. Alshareef, A. Rao, L. Solis, P. Majhi, R. Choi, B. H. Lee, G. Bersuker, and G. A. Brown, "Reliability Characteristics of Metal/High-? PMOS with Top Interface Engineered Band Offset Dielectric (BOD)," presented at IEEE International Reliability Physics Symposium, San Jose, California, 2006.

[45] B. H. Lee, S. C. Song, R. Choi, H. C. Wen, P. Majhi, P. Kirsch, C. Young, and G. Bersuker, "Challenges in implementing high-k dielectrics in the 45nm technology node,"

presented at Integrated Circuit Design and Technology, 2005. ICICDT 2005. 2005 International Conference on, 2005.

[46] Y. Senzaki, J. Gutt, G. A. Brown, P. Kirsch, H. Alshareef, K. Choi, C. Huffman, H. Wen, P. Majhi, B. H. Lee, H. Chatham, S. Park, and S. Lanee, "ALD of Advanced High-k and Metal Gate Stacks for MOS Devices," presented at 207th ECS Meeting, Quebec City, Canada, 2005.

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